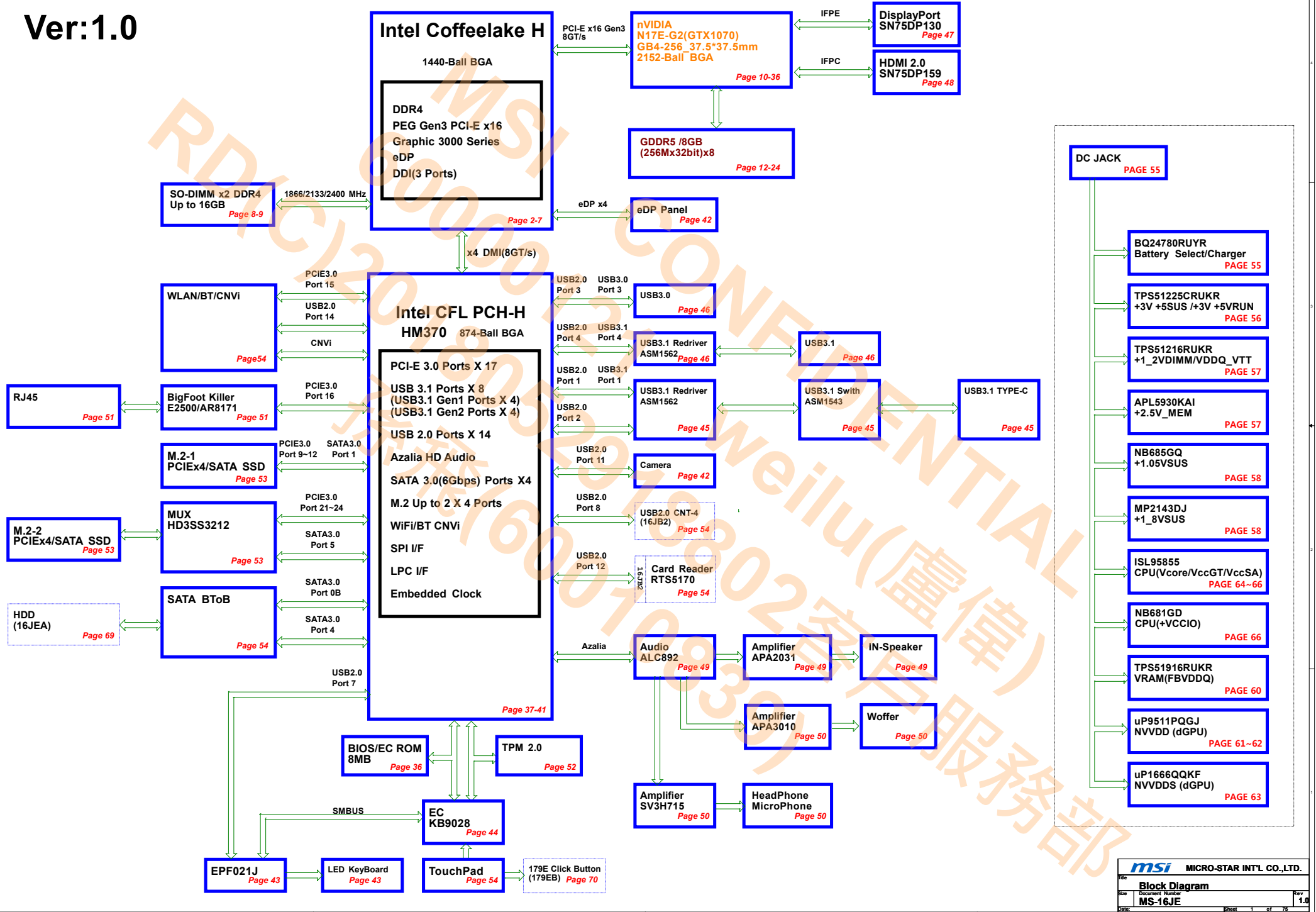
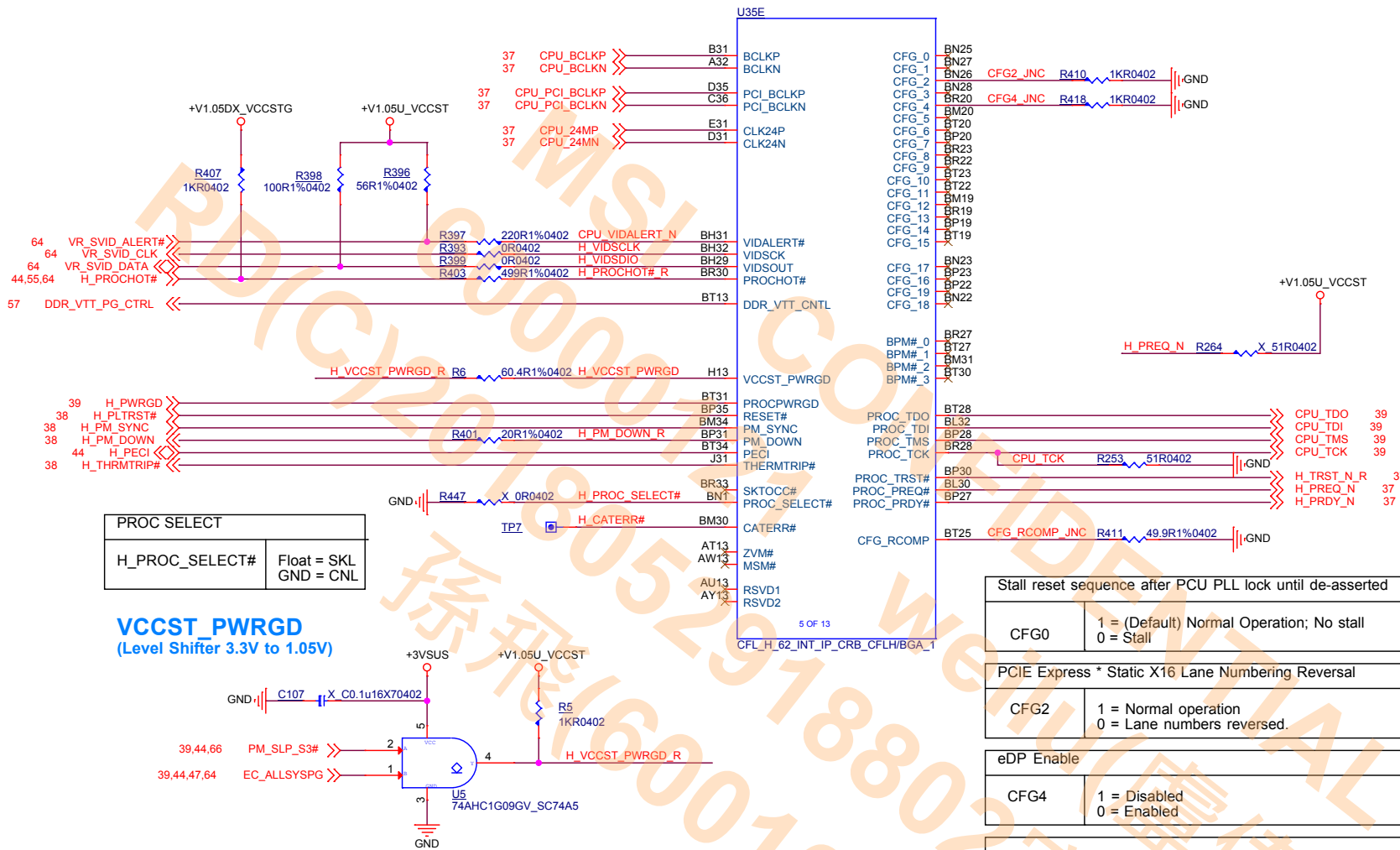


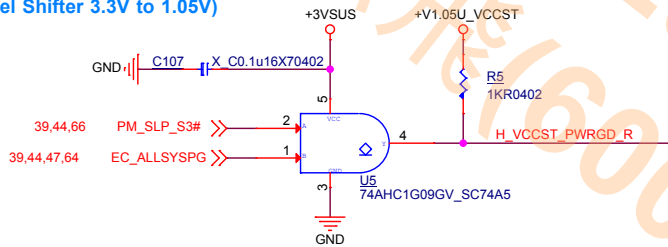
Ver:1.0





PROC SELECT	
H_PROC_SELECT#	Float = SKL GND = CNL

VCCST_PWRGD (Level Shifter 3.3V to 1.05V)



I7-8750H

I7-8750

OAD-16K5004-I06

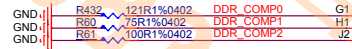
X_I7-8750

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	1 = (Default) Normal Operation; No stall 0 = Stall
PCI Express * Static X16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.
eDP Enable	
CFG4	1 = Disabled 0 = Enabled
PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*
PEG DEFER TRAINING	
CFG7	1: (default) PEG Train immediately following RESET# de assertion. 0: PEG Wait for BIOS for training

DDR Channel A

U35A			
M A DQ0	BR6	DDR0_DQ_0/DDR0_DQ_0	DDR0_CK_P_0/DDR0_CK_P_0
M A DQ1	BT6	DDR0_DQ_1/DDR0_DQ_1	DDR0_CK_N_0/DDR0_CK_N_0
M A DQ2	BP3	DDR0_DQ_2/DDR0_DQ_2	DDR0_CK_P_1/DDR0_CK_P_1
M A DQ3	BR3	DDR0_DQ_3/DDR0_DQ_3	DDR0_CK_N_1/DDR0_CK_N_1
M A DQ4	BN6	DDR0_DQ_4/DDR0_DQ_4	NC/DDR0_CK_P_2
M A DQ5	BP6	DDR0_DQ_5/DDR0_DQ_5	NC/DDR0_CK_N_2
M A DQ6	BN3	DDR0_DQ_6/DDR0_DQ_6	NC/DDR0_CK_P_3
M A DQ7	BR3	DDR0_DQ_7/DDR0_DQ_7	NC/DDR0_CK_N_3
M A DQ8	BL4	DDR0_DQ_8/DDR0_DQ_8	DDR0_CKE_0/DDR0_CKE_0
M A DQ9	BL5	DDR0_DQ_9/DDR0_DQ_9	DDR0_CKE_1/DDR0_CKE_1
M A DQ10	BL2	DDR0_DQ_10/DDR0_DQ_10	DDR0_CKE_2/DDR0_CKE_2
M A DQ11	BM1	DDR0_DQ_11/DDR0_DQ_11	DDR0_CKE_3/DDR0_CKE_3
M A DQ12	BK4	DDR0_DQ_12/DDR0_DQ_12	DDR0_CSN_0/DDR0_CSN_0
M A DQ13	BK5	DDR0_DQ_13/DDR0_DQ_13	DDR0_CSN_1/DDR0_CSN_1
M A DQ14	BK1	DDR0_DQ_14/DDR0_DQ_14	NC/DDR0_CSN_2
M A DQ15	BK2	DDR0_DQ_15/DDR0_DQ_15	NC/DDR0_CSN_3
M A DQ16	BG4	DDR0_DQ_16/DDR0_DQ_16	DDR0_ODT_0/DDR0_ODT_0
M A DQ17	BG5	DDR0_DQ_17/DDR0_DQ_17	DDR0_ODT_1/DDR0_ODT_1
M A DQ18	BF4	DDR0_DQ_18/DDR0_DQ_18	NC/DDR0_ODT_2
M A DQ19	BF5	DDR0_DQ_19/DDR0_DQ_19	NC/DDR0_ODT_3
M A DQ20	BG2	DDR0_DQ_20/DDR0_DQ_20	DDR0_CAB_4/DDR0_CAB_4
M A DQ21	BG1	DDR0_DQ_21/DDR0_DQ_21	DDR0_CAB_5/DDR0_CAB_5
M A DQ22	BF1	DDR0_DQ_22/DDR0_DQ_22	DDR0_CAB_6/DDR0_CAB_6
M A DQ23	BF2	DDR0_DQ_23/DDR0_DQ_23	DDR0_CAB_7/DDR0_CAB_7
M A DQ24	BD2	DDR0_DQ_24/DDR0_DQ_24	DDR0_CAB_8/DDR0_CAB_8
M A DQ25	BD1	DDR0_DQ_25/DDR0_DQ_25	DDR0_CAB_9/DDR0_CAB_9
M A DQ26	BD3	DDR0_DQ_26/DDR0_DQ_26	DDR0_CAB_10/DDR0_CAB_10
M A DQ27	BD5	DDR0_DQ_27/DDR0_DQ_27	DDR0_CAB_11/DDR0_CAB_11
M A DQ28	BD4	DDR0_DQ_28/DDR0_DQ_28	DDR0_CAB_12/DDR0_CAB_12
M A DQ29	BC1	DDR0_DQ_29/DDR0_DQ_29	DDR0_CAB_13/DDR0_CAB_13
M A DQ30	BC2	DDR0_DQ_30/DDR0_DQ_30	DDR0_CAB_14/DDR0_CAB_14
M A DQ31	BC3	DDR0_DQ_31/DDR0_DQ_31	DDR0_CAB_15/DDR0_CAB_15
M A DQ32	AB1	DDR0_DQ_32/DDR0_DQ_32	DDR0_CAB_16/DDR0_CAB_16
M A DQ33	AB2	DDR0_DQ_33/DDR0_DQ_33	DDR0_CAB_17/DDR0_CAB_17
M A DQ34	AA4	DDR0_DQ_34/DDR0_DQ_34	DDR0_CAB_18/DDR0_CAB_18
M A DQ35	AA5	DDR0_DQ_35/DDR0_DQ_35	DDR0_CAB_19/DDR0_CAB_19
M A DQ36	AB5	DDR0_DQ_36/DDR0_DQ_36	DDR0_CAB_20/DDR0_CAB_20
M A DQ37	AB4	DDR0_DQ_37/DDR0_DQ_37	DDR0_CAB_21/DDR0_CAB_21
M A DQ38	AA2	DDR0_DQ_38/DDR0_DQ_38	DDR0_CAB_22/DDR0_CAB_22
M A DQ39	AA1	DDR0_DQ_39/DDR0_DQ_39	DDR0_CAB_23/DDR0_CAB_23
M A DQ40	V5	DDR0_DQ_40/DDR0_DQ_40	DDR0_CAB_24/DDR0_CAB_24
M A DQ41	V2	DDR0_DQ_41/DDR0_DQ_41	DDR0_CAB_25/DDR0_CAB_25
M A DQ42	U1	DDR0_DQ_42/DDR0_DQ_42	DDR0_CAB_26/DDR0_CAB_26
M A DQ43	U2	DDR0_DQ_43/DDR0_DQ_43	DDR0_CAB_27/DDR0_CAB_27
M A DQ44	V1	DDR0_DQ_44/DDR0_DQ_44	DDR0_CAB_28/DDR0_CAB_28
M A DQ45	V4	DDR0_DQ_45/DDR0_DQ_45	DDR0_CAB_29/DDR0_CAB_29
M A DQ46	U5	DDR0_DQ_46/DDR0_DQ_46	DDR0_CAB_30/DDR0_CAB_30
M A DQ47	U4	DDR0_DQ_47/DDR0_DQ_47	DDR0_CAB_31/DDR0_CAB_31
M A DQ48	R2	DDR0_DQ_48/DDR0_DQ_48	DDR0_CAB_32/DDR0_CAB_32
M A DQ49	P5	DDR0_DQ_49/DDR0_DQ_49	DDR0_CAB_33/DDR0_CAB_33
M A DQ50	R4	DDR0_DQ_50/DDR0_DQ_50	DDR0_CAB_34/DDR0_CAB_34
M A DQ51	P4	DDR0_DQ_51/DDR0_DQ_51	DDR0_CAB_35/DDR0_CAB_35
M A DQ52	R5	DDR0_DQ_52/DDR0_DQ_52	DDR0_CAB_36/DDR0_CAB_36
M A DQ53	P2	DDR0_DQ_53/DDR0_DQ_53	DDR0_CAB_37/DDR0_CAB_37
M A DQ54	R1	DDR0_DQ_54/DDR0_DQ_54	DDR0_CAB_38/DDR0_CAB_38
M A DQ55	P1	DDR0_DQ_55/DDR0_DQ_55	DDR0_CAB_39/DDR0_CAB_39
M A DQ56	M4	DDR0_DQ_56/DDR0_DQ_56	DDR0_CAB_40/DDR0_CAB_40
M A DQ57	M1	DDR0_DQ_57/DDR0_DQ_57	DDR0_CAB_41/DDR0_CAB_41
M A DQ58	L4	DDR0_DQ_58/DDR0_DQ_58	DDR0_CAB_42/DDR0_CAB_42
M A DQ59	L2	DDR0_DQ_59/DDR0_DQ_59	DDR0_CAB_43/DDR0_CAB_43
M A DQ60	M5	DDR0_DQ_60/DDR0_DQ_60	DDR0_CAB_44/DDR0_CAB_44
M A DQ61	M2	DDR0_DQ_61/DDR0_DQ_61	DDR0_CAB_45/DDR0_CAB_45
M A DQ62	L5	DDR0_DQ_62/DDR0_DQ_62	DDR0_CAB_46/DDR0_CAB_46
M A DQ63	L1	DDR0_DQ_63/DDR0_DQ_63	DDR0_CAB_47/DDR0_CAB_47
BA2		NC/DDR0_ECC_0	DDR0_DQSN_0/DDR0_DQSN_0
BA1		NC/DDR0_ECC_1	DDR0_DQSN_1/DDR0_DQSN_1
AY6		NC/DDR0_ECC_2	DDR0_DQSN_2/DDR0_DQSN_2
BA5		NC/DDR0_ECC_3	DDR0_DQSN_3/DDR0_DQSN_3
BA6		NC/DDR0_ECC_4	DDR0_DQSN_4/DDR0_DQSN_4
AY4		NC/DDR0_ECC_5	DDR0_DQSN_5/DDR0_DQSN_5
AY3		NC/DDR0_ECC_6	DDR0_DQSN_6/DDR0_DQSN_6
AY2		NC/DDR0_ECC_7	DDR0_DQSN_7/DDR0_DQSN_7

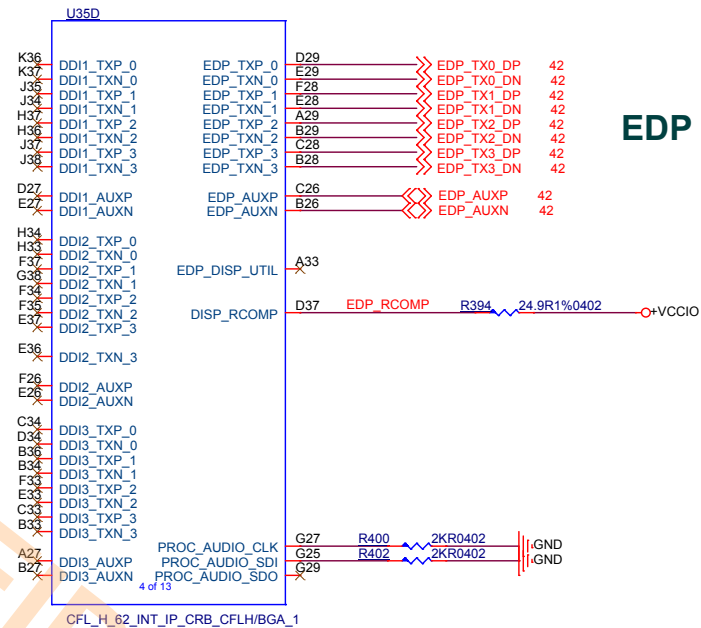
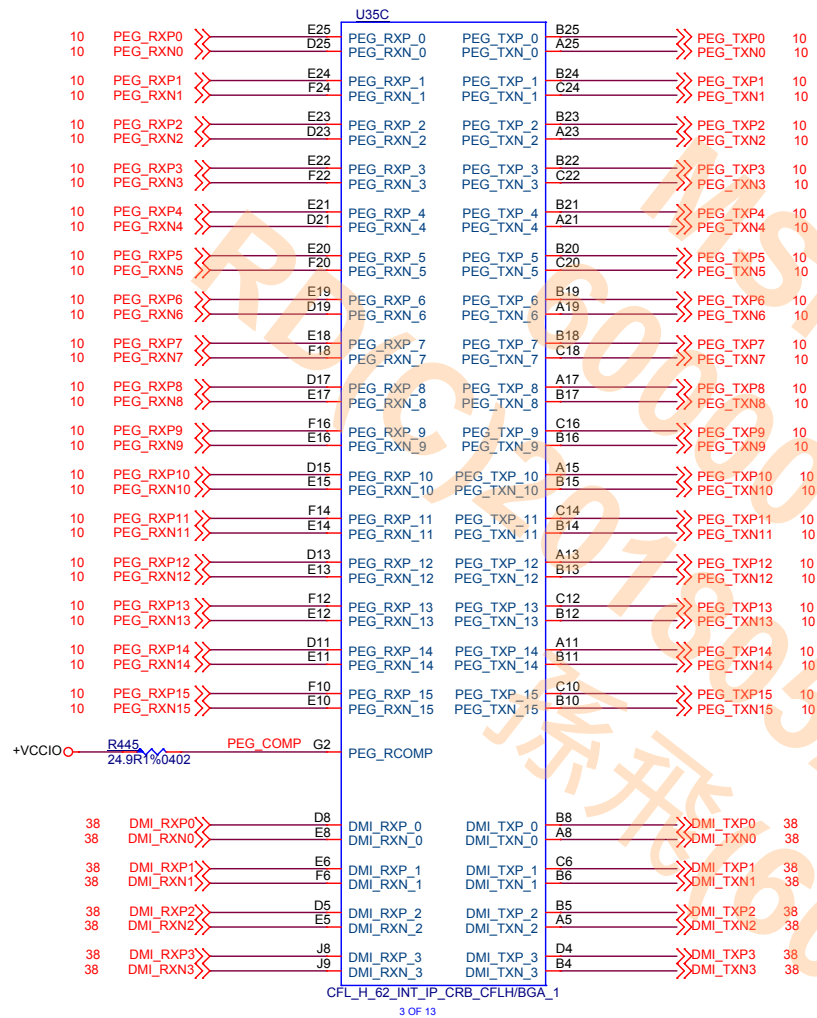
DDR CHANNEL A
CFL_H_62_INT_IP_CRB_CFLHBGA_1



DDR Channel B

U35B			
M B DQ0	BT11	DDR1_DQ_0/DDR1_DQ_0	DDR1_CK_P_0/DDR1_CK_P_0
M B DQ1	BR11	DDR1_DQ_1/DDR1_DQ_1	DDR1_CK_N_0/DDR1_CK_N_0
M B DQ2	BT9	DDR1_DQ_2/DDR1_DQ_2	DDR1_CK_P_1/DDR1_CK_P_1
M B DQ3	BR8	DDR1_DQ_3/DDR1_DQ_3	DDR1_CK_N_1/DDR1_CK_N_1
M B DQ4	BT11	DDR1_DQ_4/DDR1_DQ_4	NC/DDR1_CK_P_2
M B DQ5	BN11	DDR1_DQ_5/DDR1_DQ_5	NC/DDR1_CK_N_2
M B DQ6	BP8	DDR1_DQ_6/DDR1_DQ_6	NC/DDR1_CK_P_3
M B DQ7	BN8	DDR1_DQ_7/DDR1_DQ_7	NC/DDR1_CK_N_3
M B DQ8	BL12	DDR1_DQ_8/DDR1_DQ_8	DDR1_CKE_0/DDR1_CKE_0
M B DQ9	BL11	DDR1_DQ_9/DDR1_DQ_9	DDR1_CKE_1/DDR1_CKE_1
M B DQ10	BL8	DDR1_DQ_10/DDR1_DQ_10	DDR1_CKE_2/DDR1_CKE_2
M B DQ11	BJ8	DDR1_DQ_11/DDR1_DQ_11	DDR1_CKE_3/DDR1_CKE_3
M B DQ12	BU11	DDR1_DQ_12/DDR1_DQ_12	DDR1_CSN_0/DDR1_CSN_0
M B DQ13	BL11	DDR1_DQ_13/DDR1_DQ_13	DDR1_CSN_1/DDR1_CSN_1
M B DQ14	BL7	DDR1_DQ_14/DDR1_DQ_14	NC/DDR1_CSN_2
M B DQ15	BJ7	DDR1_DQ_15/DDR1_DQ_15	NC/DDR1_CSN_3
M B DQ16	BG11	DDR1_DQ_16/DDR1_DQ_16	DDR1_ODT_0/DDR1_ODT_0
M B DQ17	BG10	DDR1_DQ_17/DDR1_DQ_17	DDR1_ODT_1/DDR1_ODT_1
M B DQ18	BG8	DDR1_DQ_18/DDR1_DQ_18	NC/DDR1_ODT_2
M B DQ19	BF8	DDR1_DQ_19/DDR1_DQ_19	NC/DDR1_ODT_3
M B DQ20	BF11	DDR1_DQ_20/DDR1_DQ_20	DDR1_CAB_3/DDR1_CAB_3
M B DQ21	BF10	DDR1_DQ_21/DDR1_DQ_21	DDR1_CAB_4/DDR1_CAB_4
M B DQ22	BG7	DDR1_DQ_22/DDR1_DQ_22	DDR1_CAB_5/DDR1_CAB_5
M B DQ23	BF7	DDR1_DQ_23/DDR1_DQ_23	DDR1_CAB_6/DDR1_CAB_6
M B DQ24	BB11	DDR1_DQ_24/DDR1_DQ_24	DDR1_CAB_7/DDR1_CAB_7
M B DQ25	BC11	DDR1_DQ_25/DDR1_DQ_25	DDR1_CAB_8/DDR1_CAB_8
M B DQ26	BB8	DDR1_DQ_26/DDR1_DQ_26	DDR1_CAB_9/DDR1_CAB_9
M B DQ27	BC8	DDR1_DQ_27/DDR1_DQ_27	DDR1_CAB_10/DDR1_CAB_10
M B DQ28	BC10	DDR1_DQ_28/DDR1_DQ_28	DDR1_CAB_11/DDR1_CAB_11
M B DQ29	BB10	DDR1_DQ_29/DDR1_DQ_29	DDR1_CAB_12/DDR1_CAB_12
M B DQ30	BB7	DDR1_DQ_30/DDR1_DQ_30	DDR1_CAB_13/DDR1_CAB_13
M B DQ31	BB7	DDR1_DQ_31/DDR1_DQ_31	DDR1_CAB_14/DDR1_CAB_14
M B DQ32	AA11	DDR1_DQ_32/DDR1_DQ_32	DDR1_CAB_15/DDR1_CAB_15
M B DQ33	AA10	DDR1_DQ_33/DDR1_DQ_33	DDR1_CAB_16/DDR1_CAB_16
M B DQ34	AC11	DDR1_DQ_34/DDR1_DQ_34	DDR1_CAB_17/DDR1_CAB_17
M B DQ35	AC10	DDR1_DQ_35/DDR1_DQ_35	DDR1_CAB_18/DDR1_CAB_18
M B DQ36	AA7	DDR1_DQ_36/DDR1_DQ_36	DDR1_CAB_19/DDR1_CAB_19
M B DQ37	AA8	DDR1_DQ_37/DDR1_DQ_37	DDR1_CAB_20/DDR1_CAB_20
M B DQ38	AC8	DDR1_DQ_38/DDR1_DQ_38	DDR1_CAB_21/DDR1_CAB_21
M B DQ39	AC7	DDR1_DQ_39/DDR1_DQ_39	DDR1_CAB_22/DDR1_CAB_22
M B DQ40	W8	DDR1_DQ_40/DDR1_DQ_40	DDR1_CAB_23/DDR1_CAB_23
M B DQ41	W7	DDR1_DQ_41/DDR1_DQ_41	DDR1_CAB_24/DDR1_CAB_24
M B DQ42	V10	DDR1_DQ_42/DDR1_DQ_42	DDR1_CAB_25/DDR1_CAB_25
M B DQ43	V11	DDR1_DQ_43/DDR1_DQ_43	DDR1_CAB_26/DDR1_CAB_26
M B DQ44	W11	DDR1_DQ_44/DDR1_DQ_44	DDR1_CAB_27/DDR1_CAB_27
M B DQ45	W10	DDR1_DQ_45/DDR1_DQ_45	DDR1_CAB_28/DDR1_CAB_28
M B DQ46	V7	DDR1_DQ_46/DDR1_DQ_46	DDR1_CAB_29/DDR1_CAB_29
M B DQ47	V8	DDR1_DQ_47/DDR1_DQ_47	DDR1_CAB_30/DDR1_CAB_30
M B DQ48	R11	DDR1_DQ_48/DDR1_DQ_48	DDR1_CAB_31/DDR1_CAB_31
M B DQ49	P11	DDR1_DQ_49/DDR1_DQ_49	DDR1_CAB_32/DDR1_CAB_32
M B DQ50	P7	DDR1_DQ_50/DDR1_DQ_50	DDR1_CAB_33/DDR1_CAB_33
M B DQ51	R8	DDR1_DQ_51/DDR1_DQ_51	DDR1_CAB_34/DDR1_CAB_34
M B DQ52	P10	DDR1_DQ_52/DDR1_DQ_52	DDR1_CAB_35/DDR1_CAB_35
M B DQ53	P10	DDR1_DQ_53/DDR1_DQ_53	DDR1_CAB_36/DDR1_CAB_36
M B DQ54	R7	DDR1_DQ_54/DDR1_DQ_54	DDR1_CAB_37/DDR1_CAB_37
M B DQ55	P8	DDR1_DQ_55/DDR1_DQ_55	DDR1_CAB_38/DDR1_CAB_38
M B DQ56	L11	DDR1_DQ_56/DDR1_DQ_56	DDR1_CAB_39/DDR1_CAB_39
M B DQ57	M11	DDR1_DQ_57/DDR1_DQ_57	DDR1_CAB_40/DDR1_CAB_40
M B DQ58	L7	DDR1_DQ_58/DDR1_DQ_58	DDR1_CAB_41/DDR1_CAB_41
M B DQ59	M8	DDR1_DQ_59/DDR1_DQ_59	DDR1_CAB_42/DDR1_CAB_42
M B DQ60	L10	DDR1_DQ_60/DDR1_DQ_60	DDR1_CAB_43/DDR1_CAB_43
M B DQ61	M10	DDR1_DQ_61/DDR1_DQ_61	DDR1_CAB_44/DDR1_CAB_44
M B DQ62	L7	DDR1_DQ_62/DDR1_DQ_62	DDR1_CAB_45/DDR1_CAB_45
M B DQ63	M8	DDR1_DQ_63/DDR1_DQ_63	DDR1_CAB_46/DDR1_CAB_46
AW11		NC/DDR1_ECC_0	DDR1_DQSN_0/DDR1_DQSN_0
AY11		NC/DDR1_ECC_1	DDR1_DQSN_1/DDR1_DQSN_1
AY8		NC/DDR1_ECC_2	DDR1_DQSN_2/DDR1_DQSN_2
AW8		NC/DDR1_ECC_3	DDR1_DQSN_3/DDR1_DQSN_3
AY10		NC/DDR1_ECC_4	DDR1_DQSN_4/DDR1_DQSN_4
AW10		NC/DDR1_ECC_5	DDR1_DQSN_5/DDR1_DQSN_5
AY2		NC/DDR1_ECC_6	DDR1_DQSN_6/DDR1_DQSN_6
AW2		NC/DDR1_ECC_7	DDR1_DQSN_7/DDR1_DQSN_7

DDR CHANNEL B
CFL_H_62_INT_IP_CRB_CFLHBGA_1





Follow CRB v0.7
+VCCCORE
3 x 220uF POSCAP
12 x 22uF 0603
42 x 10uF 0402
48 x 1uF 0201

A10	VSS_1	VSS_82	AL10	VSS_1
A12	VSS_2	VSS_83	AL12	VSS_2
A16	VSS_3	VSS_84	AL16	VSS_3
A18	VSS_4	VSS_85	AL18	VSS_4
A20	VSS_5	VSS_86	AL20	VSS_5
A22	VSS_6	VSS_87	AL22	VSS_6
A24	VSS_7	VSS_88	AL24	VSS_7
A26	VSS_8	VSS_89	AL26	VSS_8
A28	VSS_9	VSS_90	AL28	VSS_9
A30	VSS_10	VSS_91	AL30	VSS_10
A6	VSS_11	VSS_92	AM1	VSS_11
A9	VSS_12	VSS_93	AM12	VSS_12
AA12	VSS_13	VSS_94	AM2	VSS_13
AA29	VSS_14	VSS_95	AM3	VSS_14
AA30	VSS_15	VSS_96	AM37	VSS_15
AB33	VSS_16	VSS_97	AM4	VSS_16
AB6	VSS_17	VSS_98	AM5	VSS_17
AC1	VSS_18	VSS_99	AN12	VSS_18
AC12	VSS_19	VSS_100	AN29	VSS_19
AC2	VSS_20	VSS_101	AN30	VSS_20
AC3	VSS_21	VSS_102	AN5	VSS_21
AC37	VSS_22	VSS_103	AN6	VSS_22
AC38	VSS_23	VSS_104	AP10	VSS_23
AC4	VSS_24	VSS_105	AP11	VSS_24
AC5	VSS_25	VSS_106	AP12	VSS_25
AC6	VSS_26	VSS_107	AP33	VSS_26
AD10	VSS_27	VSS_108	AP34	VSS_27
AD11	VSS_28	VSS_109	AP8	VSS_28
AD12	VSS_29	VSS_110	AP9	VSS_29
AD29	VSS_30	VSS_111	AR1	VSS_30
AD30	VSS_31	VSS_112	AR13	VSS_31
AD6	VSS_32	VSS_113	AR14	VSS_32
AD8	VSS_33	VSS_114	AR2	VSS_33
AD9	VSS_34	VSS_115	AR29	VSS_34
AE33	VSS_35	VSS_116	AR3	VSS_35
AE34	VSS_36	VSS_117	AR30	VSS_36
AE6	VSS_37	VSS_118	AR31	VSS_37
AF1	VSS_38	VSS_119	AR32	VSS_38
AF12	VSS_39	VSS_120	AR33	VSS_39
AF13	VSS_40	VSS_121	AR34	VSS_40
AF14	VSS_41	VSS_122	AR35	VSS_41
AF2	VSS_42	VSS_123	AR36	VSS_42
AF3	VSS_43	VSS_124	AR37	VSS_43
AF4	VSS_44	VSS_125	AR38	VSS_44
AG10	VSS_45	VSS_126	AR4	VSS_45
AG11	VSS_46	VSS_127	AR5	VSS_46
AG13	VSS_47	VSS_128	AT29	VSS_47
AG29	VSS_48	VSS_129	AT30	VSS_48
AG30	VSS_49	VSS_130	AT6	VSS_49
AG6	VSS_50	VSS_131	AU10	VSS_50
AG7	VSS_51	VSS_132	AU11	VSS_51
AG8	VSS_52	VSS_133	AU12	VSS_52
AH12	VSS_53	VSS_134	AU33	VSS_53
AH13	VSS_54	VSS_135	AU34	VSS_54
AH34	VSS_55	VSS_136	AU6	VSS_55
AH35	VSS_56	VSS_137	AU7	VSS_56
AH36	VSS_57	VSS_138	AU8	VSS_57
AH6	VSS_58	VSS_139	AU9	VSS_58
AJ1	VSS_59	VSS_140	AV37	VSS_59
AJ13	VSS_60	VSS_141	AV38	VSS_60
AJ2	VSS_61	VSS_142	AW1	VSS_61
AJ3	VSS_62	VSS_143	AW12	VSS_62
AJ37	VSS_63	VSS_144	AW2	VSS_63
AJ38	VSS_64	VSS_145	AW29	VSS_64
AJ4	VSS_65	VSS_146	AW3	VSS_65
AJ5	VSS_66	VSS_147	AW30	VSS_66
AJ6	VSS_67	VSS_148	AW4	VSS_67
W4	VSS_68	VSS_149	U6	VSS_68
W5	VSS_69	VSS_150	V12	VSS_69
W6	VSS_70	VSS_151	V29	VSS_70
Y10	VSS_71	VSS_152	V30	VSS_71
Y11	VSS_72	VSS_153	V31	VSS_72
Y13	VSS_73	VSS_154	V32	VSS_73
Y14	VSS_74	VSS_155	V33	VSS_74
Y37	VSS_75	VSS_156	V6	VSS_75
Y7	VSS_76	VSS_157	W1	VSS_76
Y8	VSS_77	VSS_158	W12	VSS_77
Y9	VSS_78	VSS_159	W2	VSS_78
Y9	VSS_79	VSS_160	W3	VSS_79
AK29	VSS_80	VSS_161	W33	VSS_80
AK30	VSS_81	VSS_162	W34	VSS_81

CFL_H_62!INT_IP_CRB_CFLH/BGA_1

AV5	VSS_163	VSS_244	BU15	VSS_163
AY12	VSS_164	VSS_245	BU18	VSS_164
AY34	VSS_165	VSS_246	BJ22	VSS_165
B9	VSS_166	VSS_247	BJ25	VSS_166
BA10	VSS_167	VSS_248	BJ29	VSS_167
BA11	VSS_168	VSS_249	BJ30	VSS_168
BA12	VSS_169	VSS_250	BJ31	VSS_169
BA37	VSS_170	VSS_251	BJ32	VSS_170
BA38	VSS_171	VSS_252	BJ33	VSS_171
BA6	VSS_172	VSS_253	BJ34	VSS_172
BA7	VSS_173	VSS_254	BJ35	VSS_173
BA8	VSS_174	VSS_255	BJ36	VSS_174
BA9	VSS_175	VSS_256	BK13	VSS_175
BB1	VSS_176	VSS_257	BK14	VSS_176
BB12	VSS_177	VSS_258	BK15	VSS_177
BB2	VSS_178	VSS_259	BK16	VSS_178
BB29	VSS_179	VSS_260	BK22	VSS_179
BB3	VSS_180	VSS_261	BK25	VSS_180
BB30	VSS_181	VSS_262	BK6	VSS_181
BB4	VSS_182	VSS_263	BL13	VSS_182
BB5	VSS_183	VSS_264	BL14	VSS_183
BB6	VSS_184	VSS_265	BL19	VSS_184
BC12	VSS_185	VSS_266	BL20	VSS_185
BC13	VSS_186	VSS_267	BL21	VSS_186
BC14	VSS_187	VSS_268	BL22	VSS_187
BC33	VSS_188	VSS_269	BL29	VSS_188
BC34	VSS_189	VSS_270	BL33	VSS_189
BC6	VSS_190	VSS_271	BL35	VSS_190
BD10	VSS_191	VSS_272	BL38	VSS_191
BD11	VSS_192	VSS_273	BM1	VSS_192
BD12	VSS_193	VSS_274	BM12	VSS_193
BD37	VSS_194	VSS_275	BM13	VSS_194
BD6	VSS_195	VSS_276	BM14	VSS_195
BD7	VSS_196	VSS_277	BM18	VSS_196
BD8	VSS_197	VSS_278	BM2	VSS_197
BD9	VSS_198	VSS_279	BM21	VSS_198
BE1	VSS_199	VSS_280	BM22	VSS_199
BE2	VSS_200	VSS_281	BM23	VSS_200
BE29	VSS_201	VSS_282	BM24	VSS_201
BE3	VSS_202	VSS_283	BM25	VSS_202
BE34	VSS_203	VSS_284	BM26	VSS_203
BE4	VSS_204	VSS_285	BM27	VSS_204
BE5	VSS_205	VSS_286	BM28	VSS_205
BE6	VSS_206	VSS_287	BM29	VSS_206
BF12	VSS_207	VSS_288	BM3	VSS_207
BF33	VSS_208	VSS_289	BM33	VSS_208
BF34	VSS_209	VSS_290	BM35	VSS_209
BF6	VSS_210	VSS_291	BM38	VSS_210
BG12	VSS_211	VSS_292	BM5	VSS_211
BG13	VSS_212	VSS_293	BM6	VSS_212
BG14	VSS_213	VSS_294	BM7	VSS_213
BG37	VSS_214	VSS_295	BM8	VSS_214
BG38	VSS_215	VSS_296	BM9	VSS_215
BG6	VSS_216	VSS_297	BM12	VSS_216
BH1	VSS_217	VSS_298	BM14	VSS_217
BH10	VSS_218	VSS_299	BM18	VSS_218
BH11	VSS_219	VSS_300	BM19	VSS_219
BH12	VSS_220	VSS_301	BN2	VSS_220
BH14	VSS_221	VSS_302	BN20	VSS_221
BH2	VSS_222	VSS_303	BN21	VSS_222
BH3	VSS_223	VSS_304	BN24	VSS_223
BH4	VSS_224	VSS_305	BN25	VSS_224
BH5	VSS_225	VSS_306	BN30	VSS_225
BH6	VSS_226	VSS_307	BN31	VSS_226
BH7	VSS_227	VSS_308	BN34	VSS_227
BH8	VSS_228	VSS_309	P38	VSS_228
BH9	VSS_229	VSS_310	P6	VSS_229
T2	VSS_230	VSS_311	R12	VSS_230
T3	VSS_231	VSS_312	R29	VSS_231
T34	VSS_232	VSS_313	R30	VSS_232
T35	VSS_233	VSS_314	R31	VSS_233
T36	VSS_234	VSS_315	R32	VSS_234
T5	VSS_235	VSS_316	R33	VSS_235
T7	VSS_236	VSS_317	T1	VSS_236
T8	VSS_237	VSS_318	T10	VSS_237
T9	VSS_238	VSS_319	T11	VSS_238
U37	VSS_239	VSS_320	T12	VSS_239
U38	VSS_240	VSS_321	T13	VSS_240
U39	VSS_241	VSS_322	T14	VSS_241
BJ12	VSS_242	VSS_323		
BJ14	VSS_243	VSS_324		

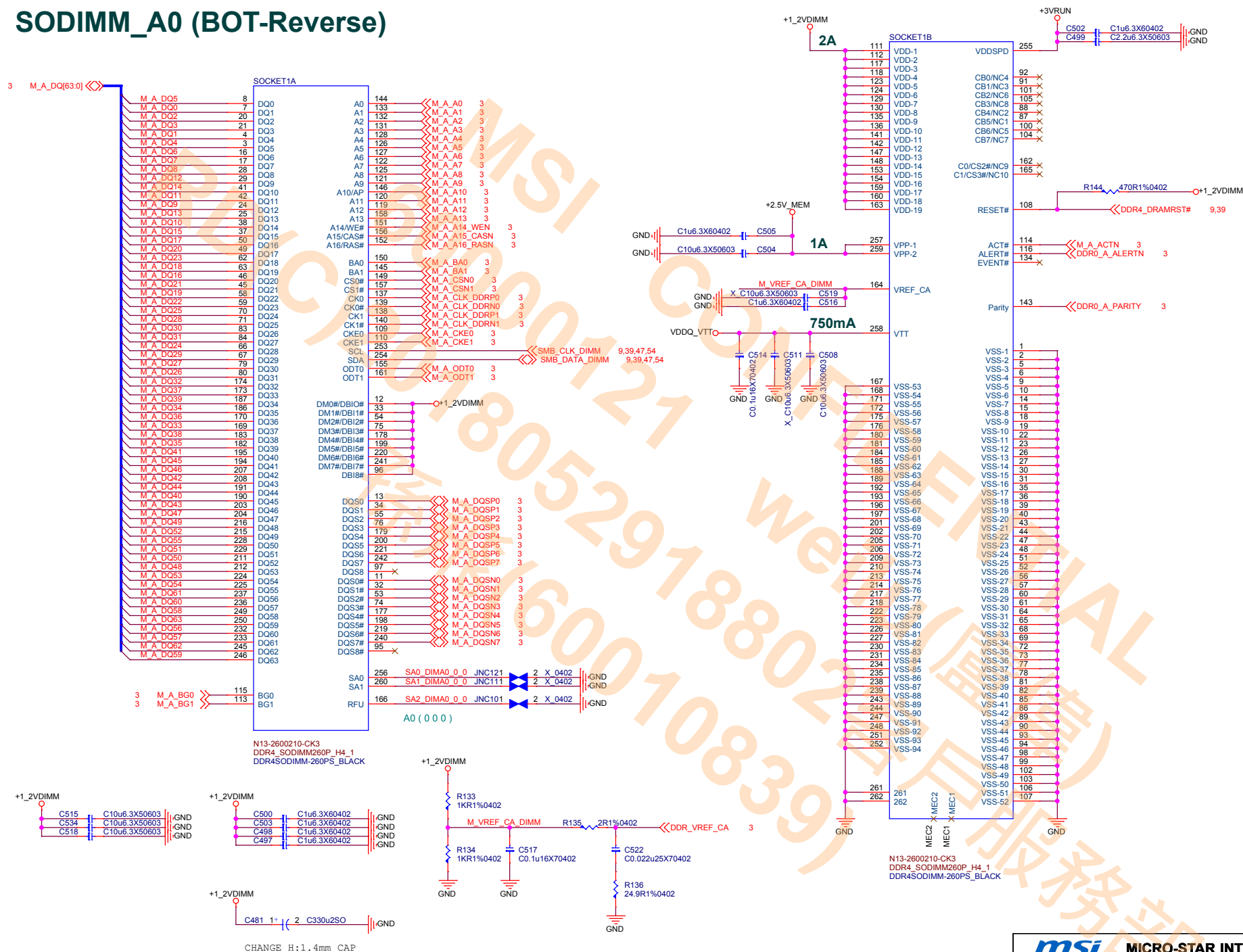
CFL_H_62!INT_IP_CRB_CFLH/BGA_1

BN4	VSS_325	VSS_409	F15	VSS_325
BN7	VSS_326	VSS_410	F17	VSS_326
BP12	VSS_327	VSS_411	F19	VSS_327
BP14	VSS_328	VSS_412	F2	VSS_328
BP18	VSS_329	VSS_413	F21	VSS_329
BP21	VSS_330	VSS_414	F23	VSS_330
BP24	VSS_331	VSS_415	F25	VSS_331
BP25	VSS_332	VSS_416	F27	VSS_332
BP26	VSS_333	VSS_417	F29	VSS_333
BP29	VSS_334	VSS_418	F3	VSS_334
BP33	VSS_335	VSS_419	F31	VSS_335
BP34	VSS_336	VSS_420	F36	VSS_336
BP7	VSS_337	VSS_421	F4	VSS_337
BR12	VSS_338	VSS_422	F5	VSS_338
BR14	VSS_339	VSS_423	F8	VSS_339
BR18	VSS_340	VSS_424	F9	VSS_340
BR21	VSS_341	VSS_425	G10	VSS_341
BR24	VSS_342	VSS_426	G12	VSS_342
BR25	VSS_343	VSS_427	G14	VSS_343
BR26	VSS_344	VSS_428	G16	VSS_344
BR29	VSS_345	VSS_429	G18	VSS_345
BR34	VSS_346	VSS_430	G20	VSS_346
BR36	VSS_347	VSS_431	G22	VSS_347
BT12	VSS_348	VSS_432	G24	VSS_348
BT14	VSS_349	VSS_433	G26	VSS_349
BT18	VSS_350	VSS_434	G28	VSS_350
BT21	VSS_351	VSS_435	G4	VSS_351
BT24	VSS_352	VSS_436	G5	VSS_352
BT29	VSS_353	VSS_437	G6	VSS_353
BT36	VSS_354	VSS_438	G8	VSS_354
BT6	VSS_355	VSS_439	G9	VSS_355
BT5	VSS_356	VSS_440	H11	VSS_356
C11	VSS_357	VSS_441	H12	VSS_357
C13	VSS_358	VSS_442	H18	VSS_358
C15	VSS_359	VSS_443	H22	VSS_359
C17	VSS_360	VSS_444	H25	VSS_360
C19	VSS_361	VSS_445	H32	VSS_361
C21	VSS_362	VSS_446	H35	VSS_362
C23	VSS_363	VSS_447	J10	VSS_363
C24	VSS_364	VSS_448	J16	VSS_364
C27	VSS_365	VSS_449	J22	VSS_365
C29	VSS_366	VSS_450	J25	VSS_366
C31	VSS_367	VSS_451	J32	VSS_367
C33	VSS_368	VSS_452	J33	VSS_368
C37	VSS_369	VSS_453	J36	VSS_369
C5	VSS_370	VSS_454	J4	VSS_370
C9	VSS_371	VSS_455	J7	VSS_371
D10	VSS_372	VSS_456	K10	VSS_372
D12	VSS_373	VSS_457	K11	VSS_373
D14	VSS_374	VSS_458	K2	VSS_374
D16	VSS_375	VSS_459	K3	VSS_375
D18	VSS_376	VSS_460	K4	VSS_376
D20	VSS_377	VSS_461	K5	VSS_377
D22	VSS_378	VSS_462	K7	VSS_378
D24	VSS_379	VSS_463	K8	VSS_379
D26	VSS_380	VSS_464	K9	VSS_380
D28	VSS_381	VSS_465	L29	VSS_381
D3	VSS_382	VSS_466	L30	VSS_382
D30	VSS_383	VSS_467	L33	VSS_383
D33	VSS_384	VSS_468	L34	VSS_384
D35	VSS_385	VSS_469	M12	VSS_385
D6	VSS_386	VSS_470	M13	VSS_386
D9	VSS_387	VSS_471	M10	VSS_387
E34	VSS_388	VSS_472	M12	VSS_388
E35	VSS_389	VSS_473	M13	VSS_389
E38	VSS_390	VSS_474	N10	VSS_390
E4	VSS_391	VSS_475	N11	VSS_391
E9	VSS_392	VSS_476	N12	VSS_392
N3	VSS_393	VSS_477	B18	VSS_393
N33	VSS_394	VSS_478	BR9	VSS_394
N34	VSS_395	VSS_479	A3	VSS_395
N4	VSS_396	VSS_480	A34	VSS_396
N6	VSS_397	VSS_481	A4	VSS_397
N7	VSS_398	VSS_482	B3	VSS_398
N8	VSS_399	VSS_483	B37	VSS_399
N9	VSS_400	VSS_484	B38	VSS_400
P12	VSS_401	VSS_485	B39	VSS_401
P37	VSS_402	VSS_486	B4	VSS_402
M14	VSS_403	VSS_487	B135	VSS_403
T13	VSS_404	VSS_488	B136	VSS_404
T14	VSS_405	VSS_489	B14	VSS_405
N1	VSS_406	VSS_490	B14	VSS_406
F11	VSS_407	VSS_491	C2	VSS_407
F13	VSS_408	VSS_492	D38	VSS_408

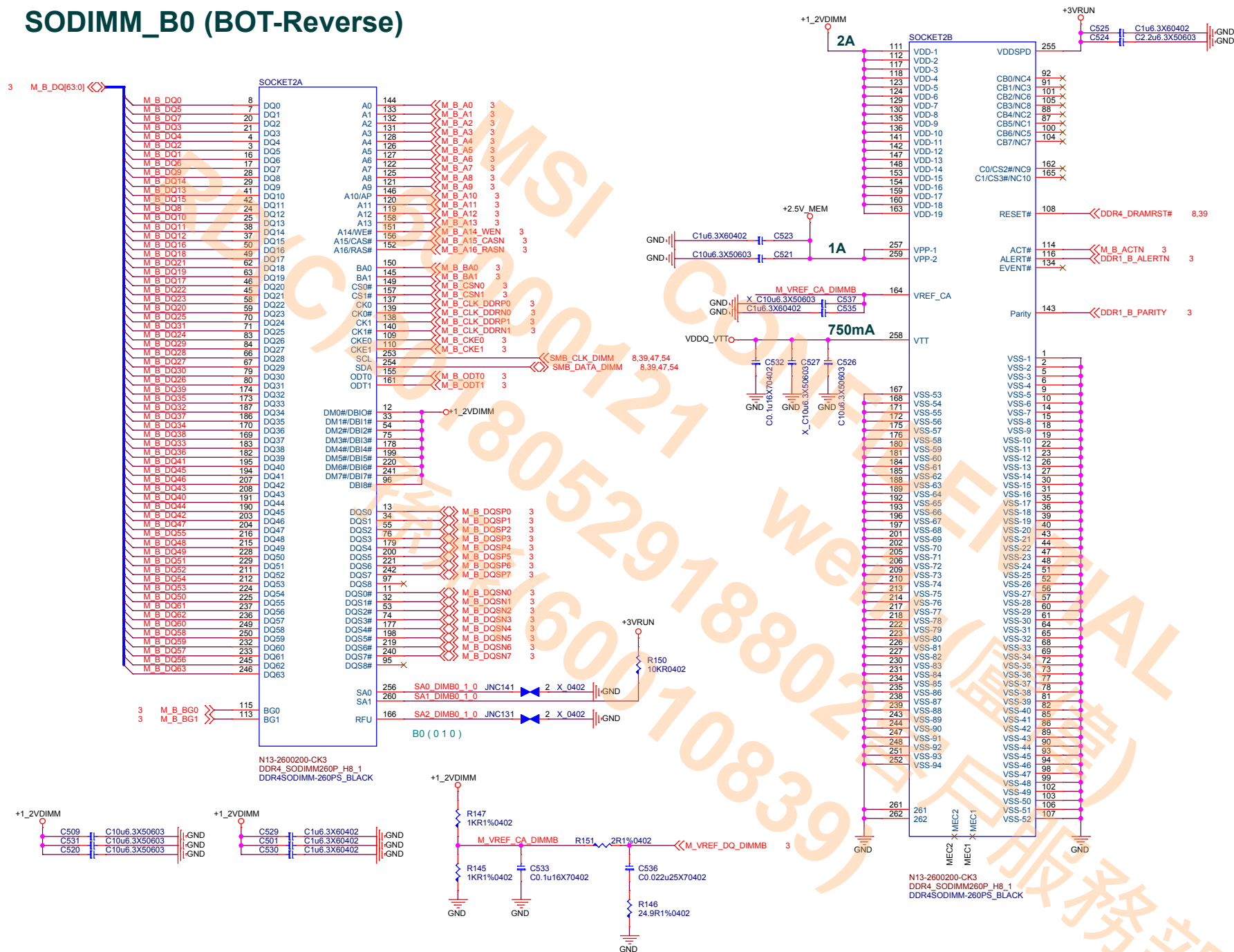
CFL_H_62!INT_IP_CRB_CFLH/BGA_1

U35F	VSS_1	VSS_82	AL10	VSS_1
U35G	VSS_2	VSS_83	AL12	VSS_2
U35H	VSS_3	VSS_84	AL16	VSS_3
U35I	VSS_4	VSS_85	AL18	VSS_4
U35J	VSS_5	VSS_86	AL20	VSS_5
U35K	VSS_6	VSS_87	AL22	VSS_6
U35L	VSS_7	VSS_88	AL24	VSS_7
U35M	VSS_8	VSS_89	AL26	VSS_8

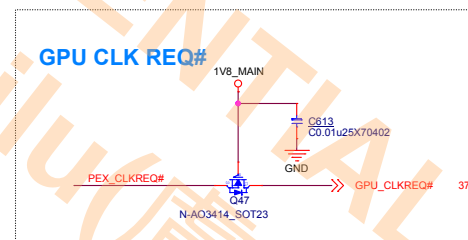
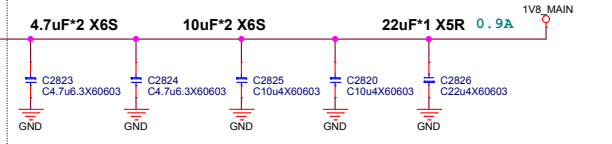
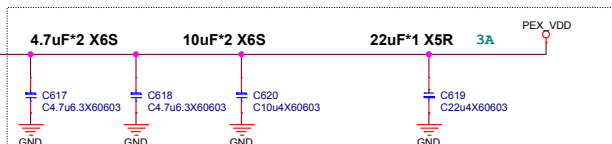
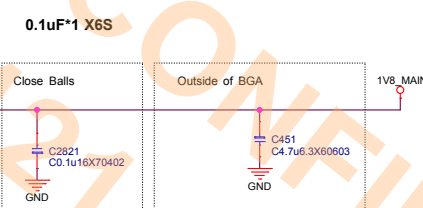
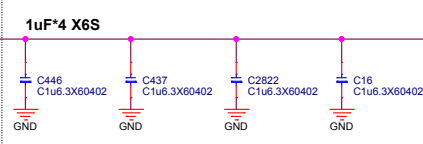
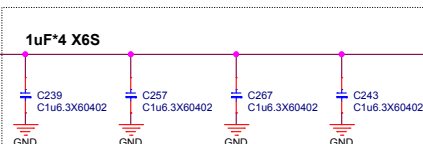
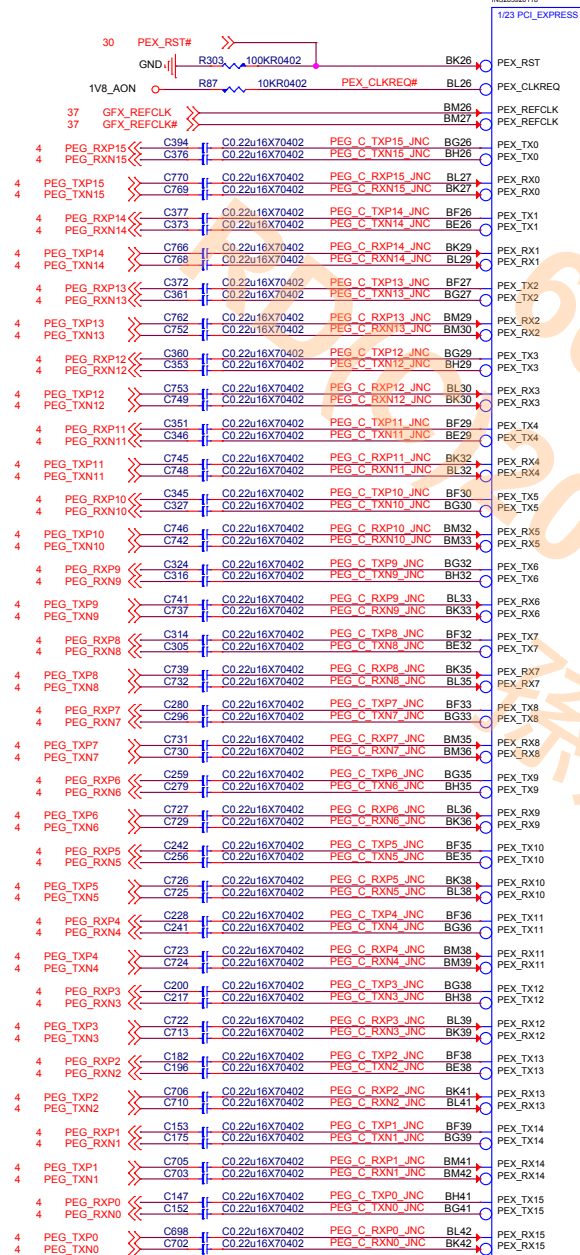
SODIMM_A0 (BOT-Reverse)




SODIMM_B0 (BOT-Reverse)



G7A
INS285020118



		MICRO-STAR INT'L CO.,LTD.	
Title DGPU PCI-E Host			
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	MS-16JE	1.0	
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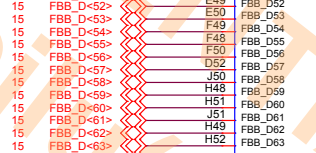
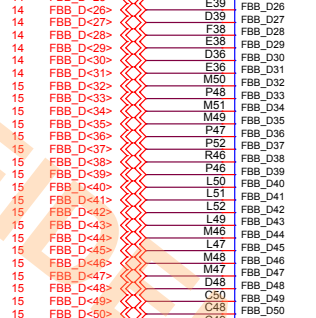
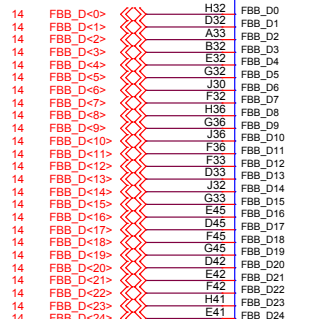
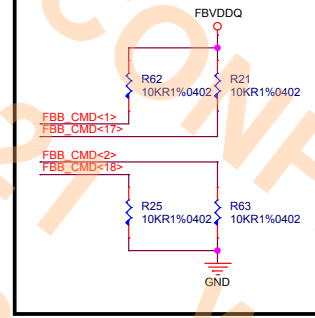
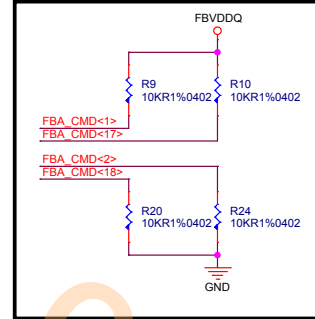
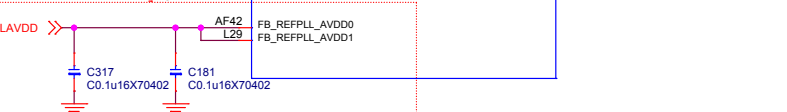
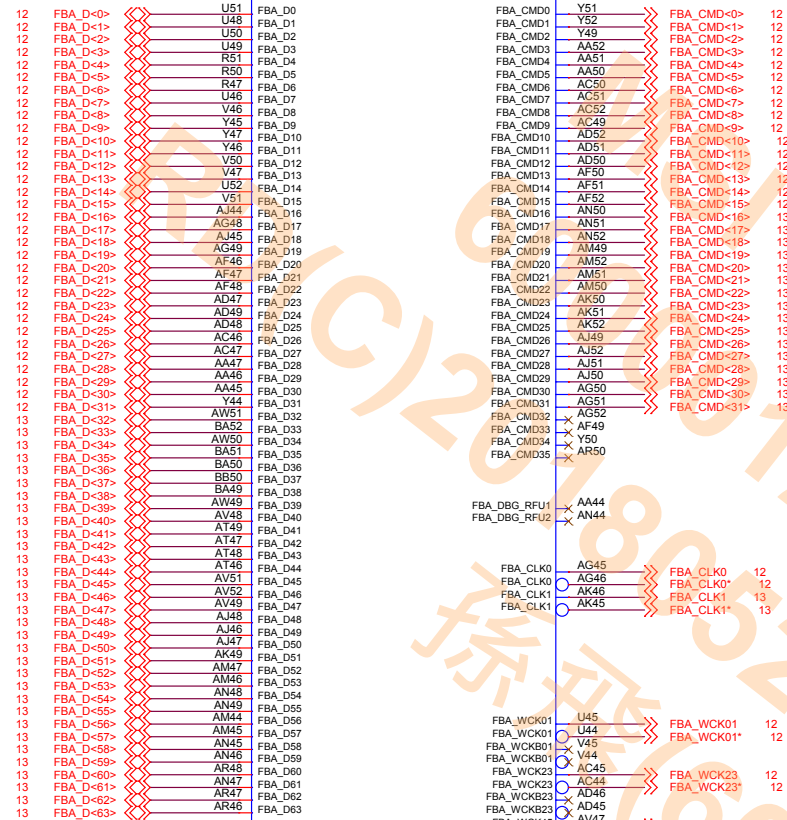
GPU Frame Buffer Partition A/B

G7B
INS285021791

2/23 FBA

G7C
INS285022041

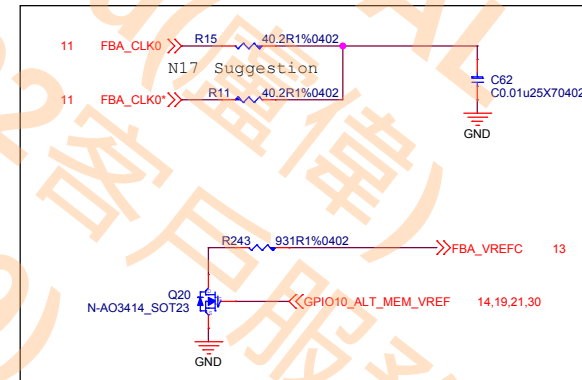
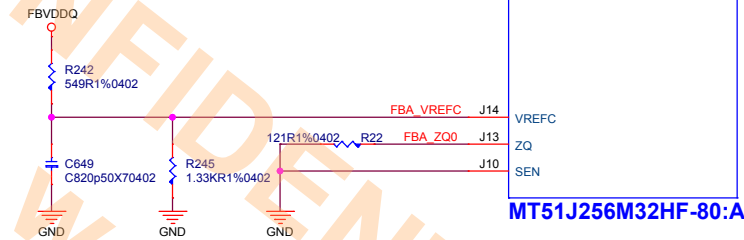
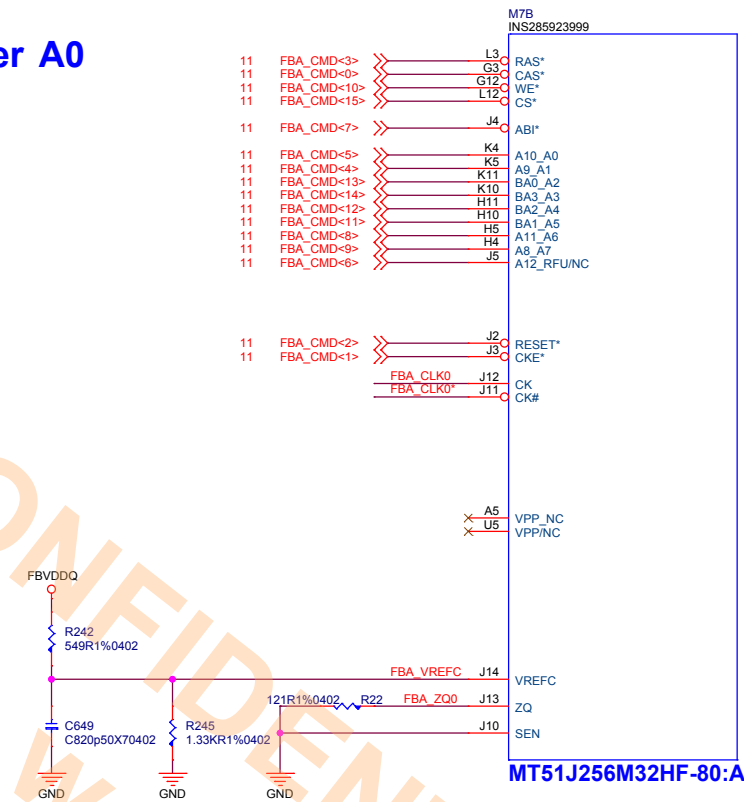
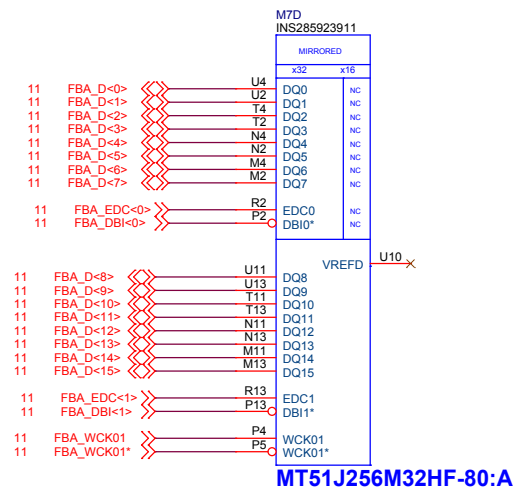
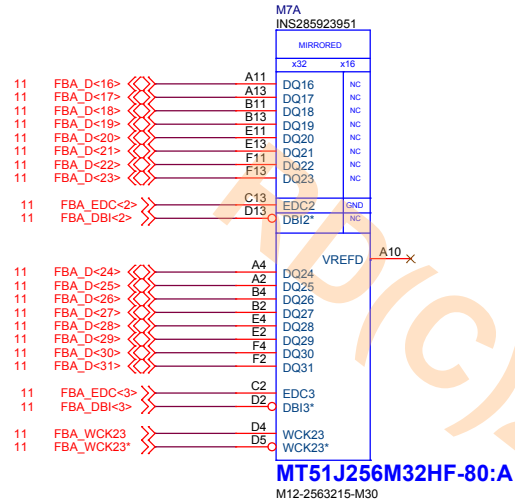
3/23 FBB



DGPU_GDDR5 FrameBuffer A0

GDD5 Command Mapping GB4-256

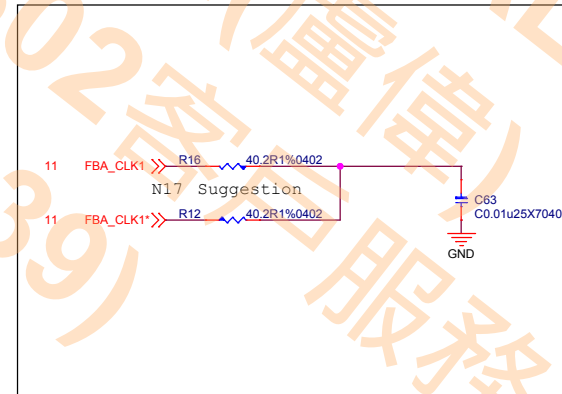
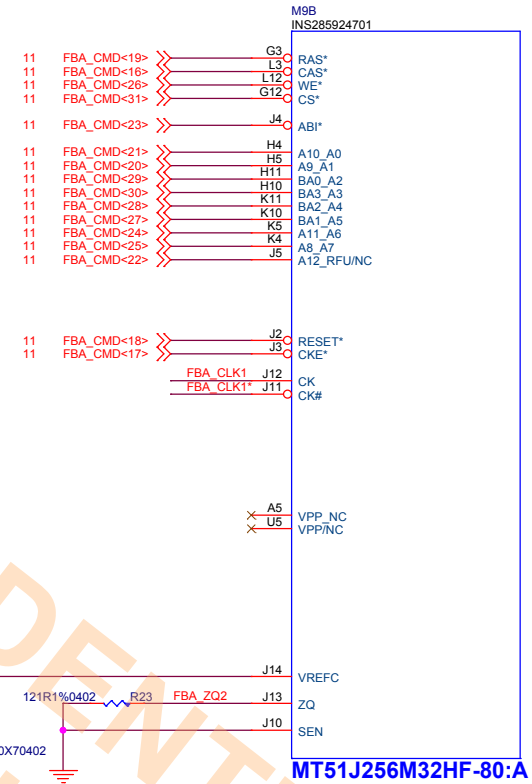
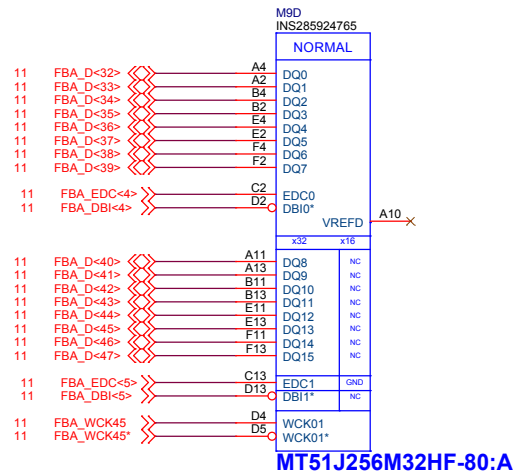
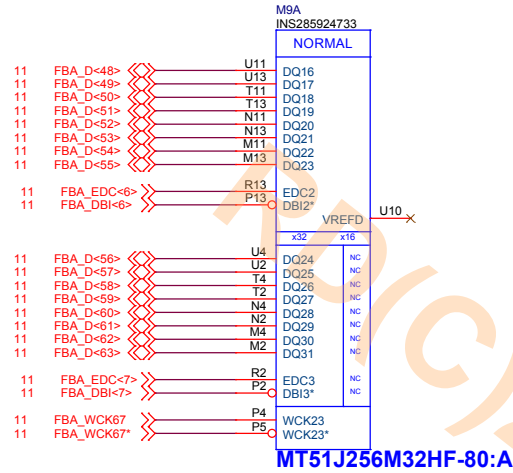
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CAS*
CMD1	CMD17	CKE*
CMD2	CMD18	RST*
CMD3	CMD19	RAS*
CMD4	CMD20	A1 A9
CMD5	CMD21	A0 A10
CMD6	CMD22	A12 RFU
CMD7	CMD23	ABI*
CMD8	CMD24	A6 A11
CMD9	CMD25	A7 A8
CMD10	CMD26	WE*
CMD11	CMD27	A5 BA1
CMD12	CMD28	A4 BA2
CMD13	CMD29	A2 BA0
CMD14	CMD30	A3 BA3
CMD15	CMD31	CS*



DGPU_GDDR5 FrameBuffer A1

GDD5 Command Mapping GB4-256

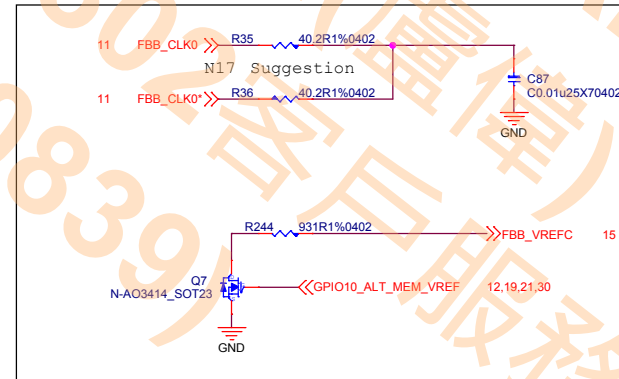
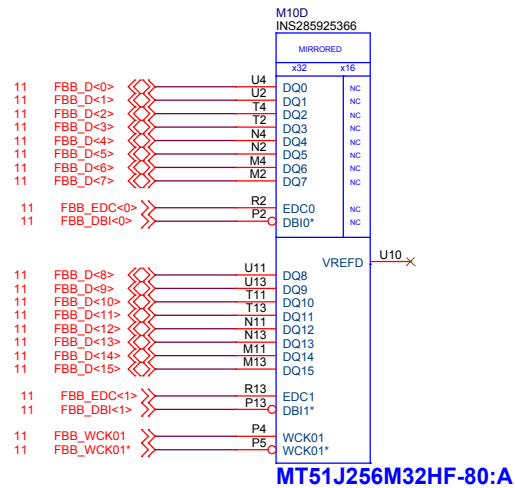
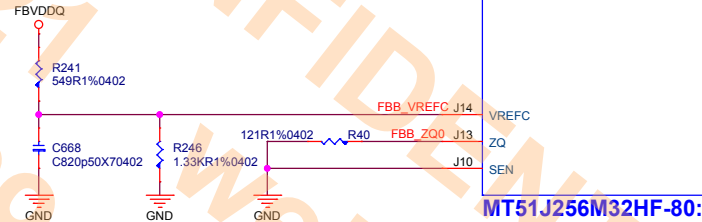
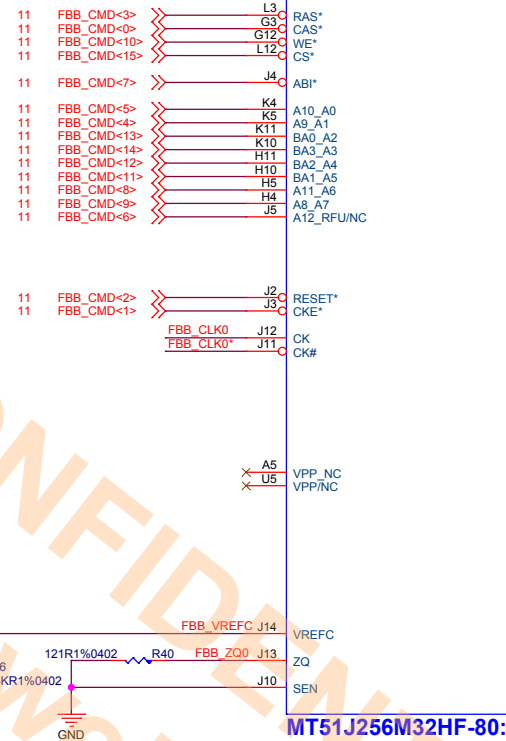
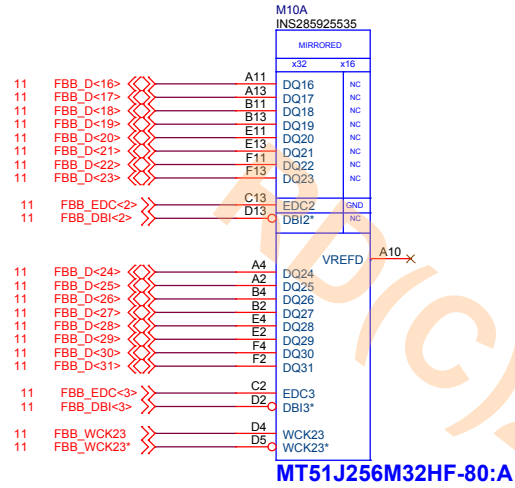
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CAS*
CMD1	CMD17	CKE*
CMD2	CMD18	RST*
CMD3	CMD19	RAS*
CMD4	CMD20	A1 A9
CMD5	CMD21	A0 A10
CMD6	CMD22	A12 RFU
CMD7	CMD23	ABI*
CMD8	CMD24	A6 A11
CMD9	CMD25	A7 A8
CMD10	CMD26	WE*
CMD11	CMD27	A5 BA1
CMD12	CMD28	A4 BA2
CMD13	CMD29	A2 BA0
CMD14	CMD30	A3 BA3
CMD15	CMD31	CS*



DGPU_GDDR5 FrameBuffer B0

GDD5 Command Mapping GB4-256

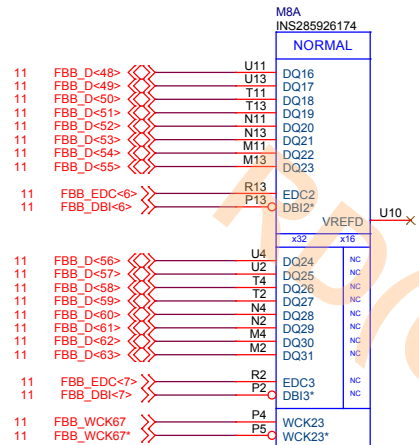
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CAS*
CMD1	CMD17	CKE*
CMD2	CMD18	RST*
CMD3	CMD19	RAS*
CMD4	CMD20	A1 A9
CMD5	CMD21	A0 A10
CMD6	CMD22	A12 RFU
CMD7	CMD23	ABI*
CMD8	CMD24	A6 A11
CMD9	CMD25	A7 A8
CMD10	CMD26	WE*
CMD11	CMD27	A5 BA1
CMD12	CMD28	A4 BA2
CMD13	CMD29	A2 BA0
CMD14	CMD30	A3 BA3
CMD15	CMD31	CS*



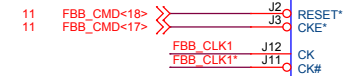
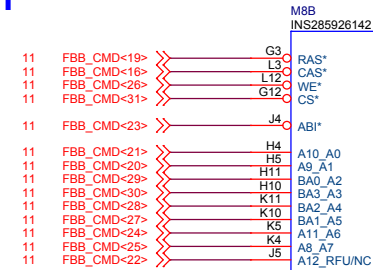
DGPU_GDDR5 FrameBuffer B1

GDD5 Command Mapping GB4-256

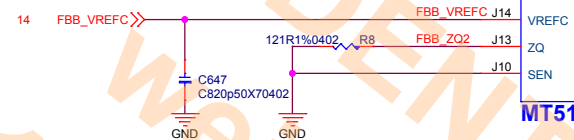
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CAS*
CMD1	CMD17	CKE*
CMD2	CMD18	RST*
CMD3	CMD19	RAS*
CMD4	CMD20	A1 A9
CMD5	CMD21	A0 A10
CMD6	CMD22	A12 RFU
CMD7	CMD23	ABI*
CMD8	CMD24	A6 A11
CMD9	CMD25	A7 A8
CMD10	CMD26	WE*
CMD11	CMD27	A5 BA1
CMD12	CMD28	A4 BA2
CMD13	CMD29	A2 BA0
CMD14	CMD30	A3 BA3
CMD15	CMD31	CS*



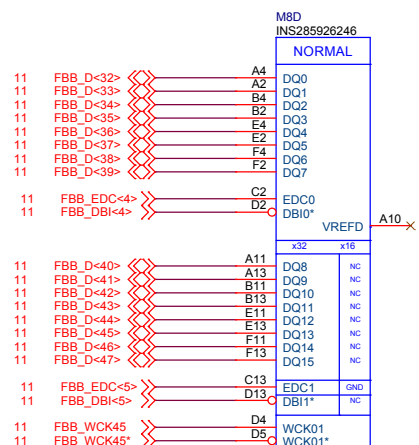
MT51J256M32HF-80:A



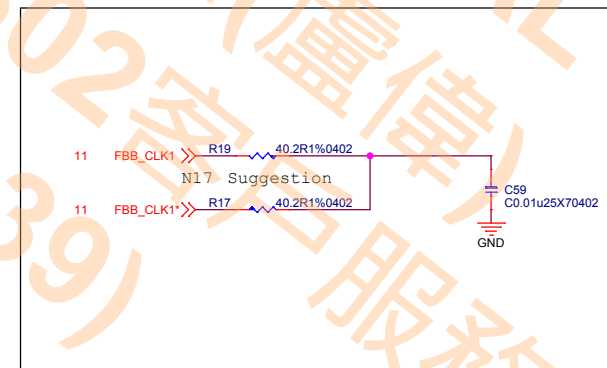
MT51J256M32HF-80:A



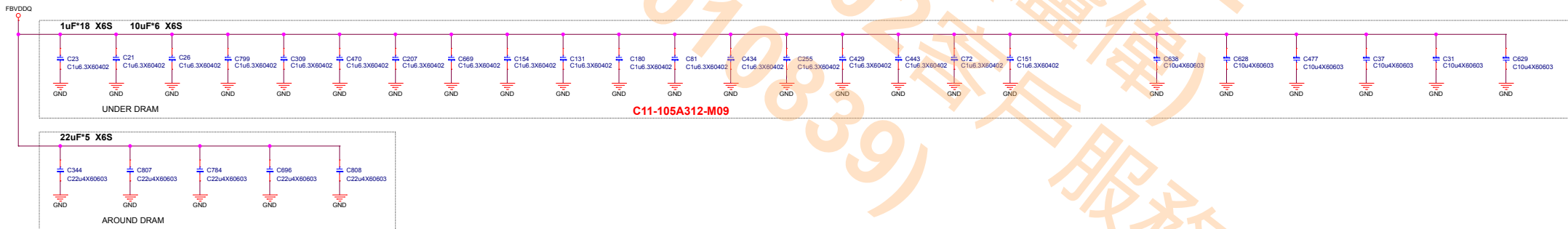
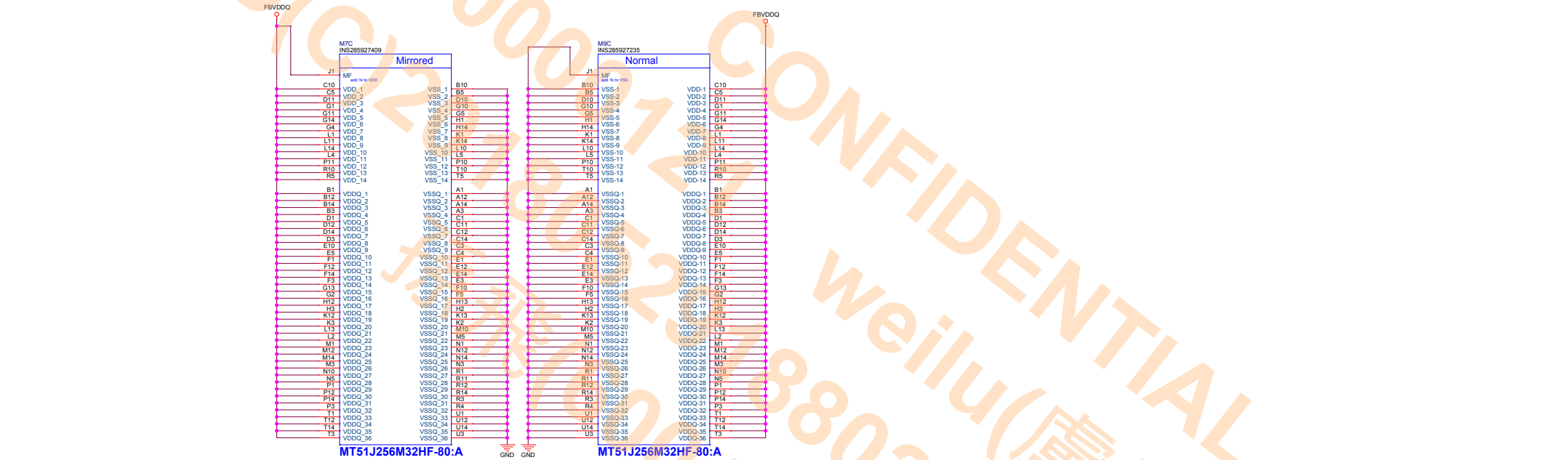
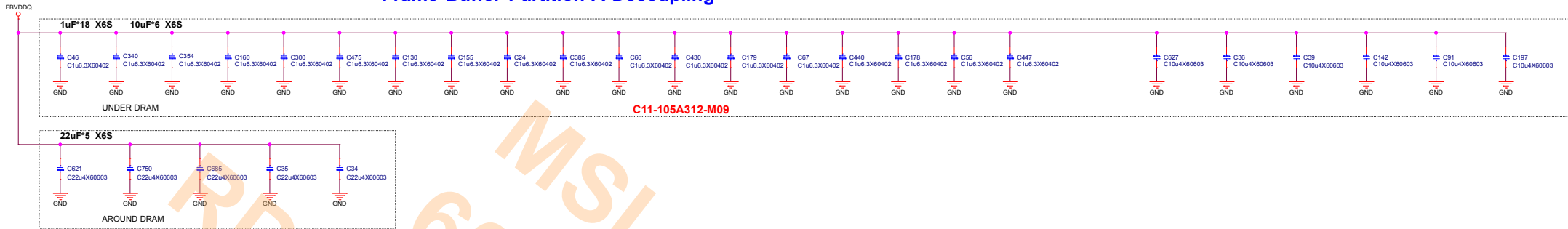
MT51J256M32HF-80:A



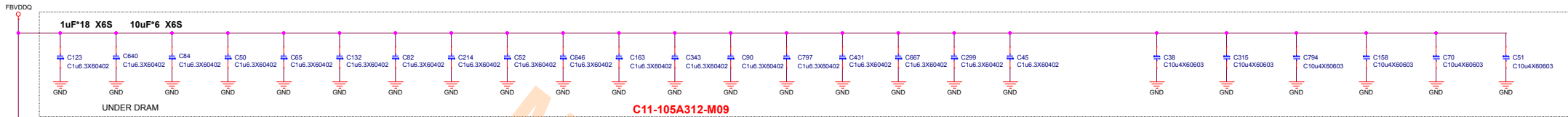
MT51J256M32HF-80:A



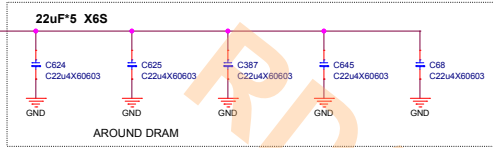
Frame Buffer Partition A Decoupling



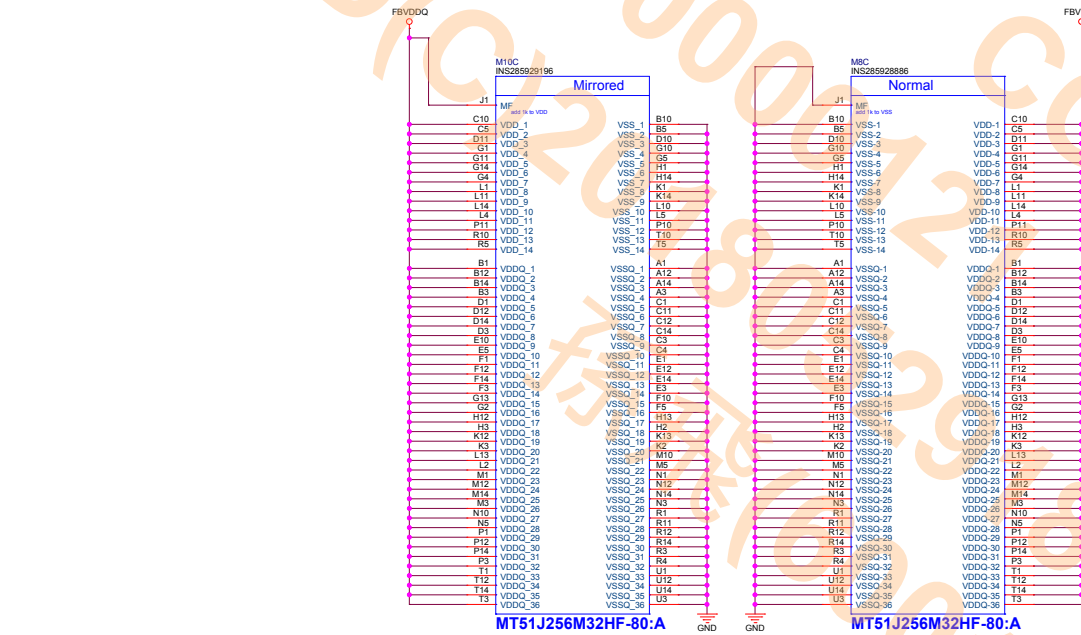
Frame Buffer Partition B Decoupling



C11-105A312-M09

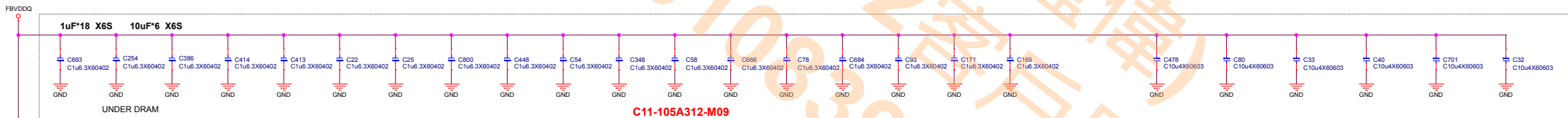


AROUND DRAM

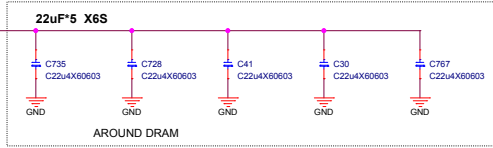


MT51J256M32HF-80:A

MT51J256M32HF-80:A



C11-105A312-M09



AROUND DRAM

GPU Frame Buffer Partition C/D

G7D
N525930177

4/23 FBC

19	FBC_D<0>	C6	FBC_D0
19	FBC_D<1>	D6	FBC_D1
19	FBC_D<2>	A6	FBC_D2
19	FBC_D<3>	B6	FBC_D3
19	FBC_D<4>	B4	FBC_D4
19	FBC_D<5>	A4	FBC_D5
19	FBC_D<6>	B3	FBC_D6
19	FBC_D<7>	C4	FBC_D7
19	FBC_D<8>	D9	FBC_D8
19	FBC_D<9>	C9	FBC_D9
19	FBC_D<10>	E9	FBC_D10
19	FBC_D<11>	B8	FBC_D11
19	FBC_D<12>	A8	FBC_D12
19	FBC_D<13>	F8	FBC_D13
19	FBC_D<14>	F6	FBC_D14
19	FBC_D<15>	E6	FBC_D15
19	FBC_D<16>	F18	FBC_D16
19	FBC_D<17>	G18	FBC_D17
19	FBC_D<18>	E18	FBC_D18
19	FBC_D<19>	H18	FBC_D19
19	FBC_D<20>	D15	FBC_D20
19	FBC_D<21>	E15	FBC_D21
19	FBC_D<22>	G17	FBC_D22
19	FBC_D<23>	H17	FBC_D23
19	FBC_D<24>	J15	FBC_D24
19	FBC_D<25>	H15	FBC_D25
19	FBC_D<26>	E14	FBC_D26
19	FBC_D<27>	F14	FBC_D27
19	FBC_D<28>	H11	FBC_D28
19	FBC_D<29>	G11	FBC_D29
19	FBC_D<30>	F11	FBC_D30
19	FBC_D<31>	E11	FBC_D31
20	FBC_D<32>	J29	FBC_D32
20	FBC_D<33>	F30	FBC_D33
20	FBC_D<34>	H29	FBC_D34
20	FBC_D<35>	G30	FBC_D35
20	FBC_D<36>	B30	FBC_D36
20	FBC_D<37>	A30	FBC_D37
20	FBC_D<38>	H30	FBC_D38
20	FBC_D<39>	C30	FBC_D39
20	FBC_D<40>	D27	FBC_D40
20	FBC_D<41>	J26	FBC_D41
20	FBC_D<42>	F27	FBC_D42
20	FBC_D<43>	G27	FBC_D43
20	FBC_D<44>	C27	FBC_D44
20	FBC_D<45>	B27	FBC_D45
20	FBC_D<46>	A27	FBC_D46
20	FBC_D<47>	G29	FBC_D47
20	FBC_D<48>	H20	FBC_D48
20	FBC_D<49>	D18	FBC_D49
20	FBC_D<50>	G20	FBC_D50
20	FBC_D<51>	E20	FBC_D51
20	FBC_D<52>	F23	FBC_D52
20	FBC_D<53>	E21	FBC_D53
20	FBC_D<54>	D21	FBC_D54
20	FBC_D<55>	E23	FBC_D55
20	FBC_D<56>	G24	FBC_D56
20	FBC_D<57>	H26	FBC_D57
20	FBC_D<58>	F24	FBC_D58
20	FBC_D<59>	G26	FBC_D59
20	FBC_D<60>	F26	FBC_D60
20	FBC_D<61>	D26	FBC_D61
20	FBC_D<62>	B26	FBC_D62
20	FBC_D<63>	C26	FBC_D63

19	FBC_DBI<0>	A5	FBC_DQM0
19	FBC_DBI<1>	C8	FBC_DQM1
19	FBC_DBI<2>	J18	FBC_DQM2
19	FBC_DBI<3>	F12	FBC_DQM3
20	FBC_DBI<4>	D29	FBC_DQM4
20	FBC_DBI<5>	E27	FBC_DQM5
20	FBC_DBI<6>	F20	FBC_DQM6
20	FBC_DBI<7>	E26	FBC_DQM7

19	FBC_EDC<0>	D5	FBC_DQS_WP0
19	FBC_EDC<1>	D8	FBC_DQS_WP1
19	FBC_EDC<2>	E17	FBC_DQS_WP2
19	FBC_EDC<3>	E12	FBC_DQS_WP3
20	FBC_EDC<4>	E30	FBC_DQS_WP4
20	FBC_EDC<5>	B29	FBC_DQS_WP5
20	FBC_EDC<6>	G21	FBC_DQS_WP6
20	FBC_EDC<7>	E24	FBC_DQS_WP7

Y25	GND
Y26	GND
Y27	GND
Y28	GND
Y29	GND
Y30	GND
Y31	GND
Y32	GND

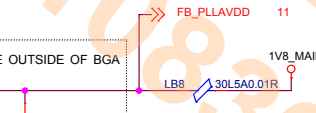
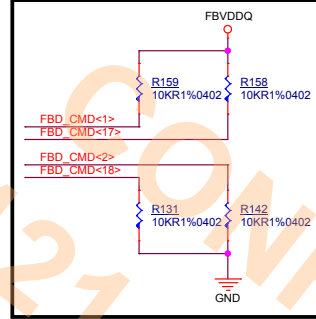
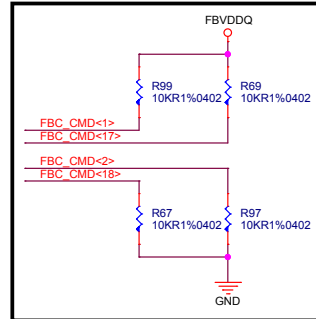
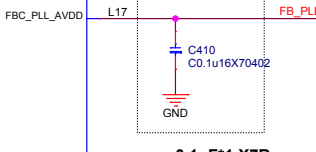
N17E-G2-A1

FBC_CMD0	C11	FBC_CMD<0>	19
FBC_CMD1	B11	FBC_CMD<1>	19
FBC_CMD2	A11	FBC_CMD<2>	19
FBC_CMD3	D11	FBC_CMD<3>	19
FBC_CMD4	A12	FBC_CMD<4>	19
FBC_CMD5	B12	FBC_CMD<5>	19
FBC_CMD6	C12	FBC_CMD<6>	19
FBC_CMD7	C14	FBC_CMD<7>	19
FBC_CMD8	B14	FBC_CMD<8>	19
FBC_CMD9	A14	FBC_CMD<9>	19
FBC_CMD10	D14	FBC_CMD<10>	19
FBC_CMD11	A15	FBC_CMD<11>	19
FBC_CMD12	C15	FBC_CMD<12>	19
FBC_CMD13	C17	FBC_CMD<13>	19
FBC_CMD14	B17	FBC_CMD<14>	19
FBC_CMD15	B24	FBC_CMD<15>	19
FBC_CMD16	A24	FBC_CMD<16>	20
FBC_CMD17	D23	FBC_CMD<17>	20
FBC_CMD18	A23	FBC_CMD<18>	20
FBC_CMD19	B23	FBC_CMD<19>	20
FBC_CMD20	C23	FBC_CMD<20>	20
FBC_CMD21	C22	FBC_CMD<21>	20
FBC_CMD22	B21	FBC_CMD<22>	20
FBC_CMD23	A21	FBC_CMD<23>	20
FBC_CMD24	D20	FBC_CMD<24>	20
FBC_CMD25	A20	FBC_CMD<25>	20
FBC_CMD26	B20	FBC_CMD<26>	20
FBC_CMD27	C20	FBC_CMD<27>	20
FBC_CMD28	C18	FBC_CMD<28>	20
FBC_CMD29	B18	FBC_CMD<29>	20
FBC_CMD30	A18	FBC_CMD<30>	20
FBC_CMD31	D17	FBC_CMD<31>	20
FBC_CMD32	A17		
FBC_CMD33	C24		

FBC_DBG_RFU1	J14
FBC_DBG_RFU2	J23

FBC_CLK0	G15	FBC_CLK0	19
FBC_CLK1	F15	FBC_CLK0*	20
FBC_CLK1*	J21	FBC_CLK1*	20

FBC_WCK01	F8	FBC_WCK01	19
FBC_WCK01*	G8	FBC_WCK01*	19
FBC_WCKB01	G9		
FBC_WCKB01*	F9		
FBC_WCK23	H12	FBC_WCK23	19
FBC_WCK23*	G12	FBC_WCK23*	19
FBC_WCKB23	G14		
FBC_WCKB23*	H14		
FBC_WCK45	J27	FBC_WCK45	20
FBC_WCK45*	H27	FBC_WCK45*	20
FBC_WCKB45	E29		
FBC_WCKB45*	G23	FBC_WCK67	20
FBC_WCK67	H23	FBC_WCK67*	20
FBC_WCKB67	H24		
FBC_WCKB67*	J24		



N17E-G2-A1

G7E
N525930338

5/23 FBD

FBD_D0	AK8	FBD_D0	21
FBD_D1	AK4	FBD_D1	21
FBD_D2	AK2	FBD_D2	21
FBD_D3	AK3	FBD_D3	21
FBD_D4	AK5	FBD_D4	21
FBD_D5	AK8	FBD_D5	21
FBD_D6	AK8	FBD_D6	21
FBD_D7	AK7	FBD_D7	21
FBD_D8	AG4	FBD_D8	21
FBD_D9	AF9	FBD_D9	21
FBD_D10	AG8	FBD_D10	21
FBD_D11	AG7	FBD_D11	21
FBD_D12	AJ4	FBD_D12	21
FBD_D13	AJ5	FBD_D13	21
FBD_D14	AJ6	FBD_D14	21
FBD_D15	AG5	FBD_D15	21
FBD_D16	Y8	FBD_D16	21
FBD_D17	Y5	FBD_D17	21
FBD_D18	V5	FBD_D18	21
FBD_D19	Y4	FBD_D19	21
FBD_D20	AA8	FBD_D20	21
FBD_D21	AA3	FBD_D21	21
FBD_D22	AC5	FBD_D22	21
FBD_D23	AC4	FBD_D23	21
FBD_D24	AD7	FBD_D24	21
FBD_D25	AD8	FBD_D25	21
FBD_D26	AF6	FBD_D26	21
FBD_D27	AD6	FBD_D27	21
FBD_D28	AF7	FBD_D28	21
FBD_D29	AF8	FBD_D29	21
FBD_D30	AF2	FBD_D30	21
FBD_D31	FBD_D31		
FBD_D32	F4	FBD_D32	21
FBD_D33	E1	FBD_D33	21
FBD_D34	F3	FBD_D34	21
FBD_D35	D2	FBD_D35	21
FBD_D36	D1	FBD_D36	21
FBD_D37	C3	FBD_D37	21
FBD_D38	C2	FBD_D38	21
FBD_D39	J5	FBD_D39	21
FBD_D40	J4	FBD_D40	21
FBD_D41	L8	FBD_D41	21
FBD_D42	J2	FBD_D42	21
FBD_D43	F1	FBD_D43	21
FBD_D44	F2	FBD_D44	21
FBD_D45	H4	FBD_D45	21
FBD_D46	H5	FBD_D46	21
FBD_D47	V7	FBD_D47	21
FBD_D48	V8	FBD_D48	21
FBD_D49	V5	FBD_D49	21
FBD_D50	V9	FBD_D50	21
FBD_D51	U4	FBD_D51	21
FBD_D52	R5	FBD_D52	21
FBD_D53	R6	FBD_D53	21
FBD_D54	U8	FBD_D54	21
FBD_D55	P6	FBD_D55	21
FBD_D56	R9	FBD_D56	21
FBD_D57	P4	FBD_D57	21
FBD_D58	P5	FBD_D58	21
FBD_D59	L7	FBD_D59	21
FBD_D60	L6	FBD_D60	21
FBD_D61	L4	FBD_D61	21
FBD_D62	L5	FBD_D62	21
FBD_D63			

FBD_DBI<0>	AG1	FBD_DQM0	21
FBD_DBI<1>	AG1	FBD_DQM1	21
FBD_DBI<2>	AD5	FBD_DQM2	21
FBD_DBI<3>	D3	FBD_DQM3	21
FBD_DBI<4>	H3	FBD_DQM4	21
FBD_DBI<5>	U5	FBD_DQM5	21
FBD_DBI<6>	M9	FBD_DQM6	21
FBD_DBI<7>	M9	FBD_DQM7	21

FBD_EDC<0>	AG2	FBD_DQS_WP0	21
FBD_EDC<1>	AA9	FBD_DQS_WP1	21
FBD_EDC<2>	AF4	FBD_DQS_WP2	21
FBD_EDC<3>	E3	FBD_DQS_WP3	21
FBD_EDC<4>	U6	FBD_DQS_WP4	21
FBD_EDC<5>	M5	FBD_DQS_WP5	21
FBD_EDC<6>	M5	FBD_DQS_WP6	21
FBD_EDC<7>	M5	FBD_DQS_WP7	21

FBD_DQS_WP0	Y33	GND
FBD_DQS_WP1	Y34	GND
FBD_DQS_WP2	Y35	GND
FBD_DQS_WP3	Y36	GND
FBD_DQS_WP4	Y37	GND
FBD_DQS_WP5	Y38	GND
FBD_DQS_WP6	Y39	GND
FBD_DQS_WP7	Y39	GND



N17E-G2-A1

FBD_CMD0	AD2	FBD_CMD<0>	21
FBD_CMD1	AD1	FBD_CMD<1>	21
FBD_CMD2	AD4	FBD_CMD<2>	21
FBD_CMD3	AC1	FBD_CMD<3>	21
FBD_CMD4	AC2	FBD_CMD<4>	21
FBD_CMD5	AC3	FBD_CMD<5>	21
FBD_CMD6	AA3	FBD_CMD<6>	21
FBD_CMD7	AA2	FBD_CMD<7>	21
FBD_CMD8	AA1	FBD_CMD<8>	21
FBD_CMD9	AA4	FBD_CMD<9>	21
FBD_CMD10	Y1	FBD_CMD<10>	21
FBD_CMD11	Y2	FBD_CMD<11>	21
FBD_CMD12	Y3	FBD_CMD<12>	21
FBD_CMD13	V3	FBD_CMD<13>	21
FBD_CMD14	V2	FBD_CMD<14>	21
FBD_CMD15	V1	FBD_CMD<15>	21
FBD_CMD16	L3	FBD_CMD<16>	22
FBD_CMD17	L2	FBD_CMD<17>	22
FBD_CMD18	L1	FBD_CMD<18>	22
FBD_CMD19	M4	FBD_CMD<19>	22
FBD_CMD20	M1	FBD_CMD<20>	22
FBD_CMD21	M2	FBD_CMD<21>	22
FBD_CMD22	M3	FBD_CMD<22>	22
FBD_CMD23	P3	FBD_CMD<23>	22
FBD_CMD24	P2	FBD_CMD<24>	22
FBD_CMD25	P1	FBD_CMD<25>	22
FBD_CMD26	R4	FBD_CMD<26>	22
FBD_CMD27	R1	FBD_CMD<27>	22
FBD_CMD28	R2	FBD_CMD<28>	22
FBD_CMD29	R3	FBD_CMD<29>	22
FBD_CMD30	U3	FBD_CMD<30>	22
FBD_CMD31	U2	FBD_CMD<31>	22
FBD_CMD32	U1		
FBD_CMD33	V4		
FBD_CMD34	AD3		
FBD_CMD35	J3		

FBD_DBG_RFU1	AC9
FBD_DBG_RFU2	P9

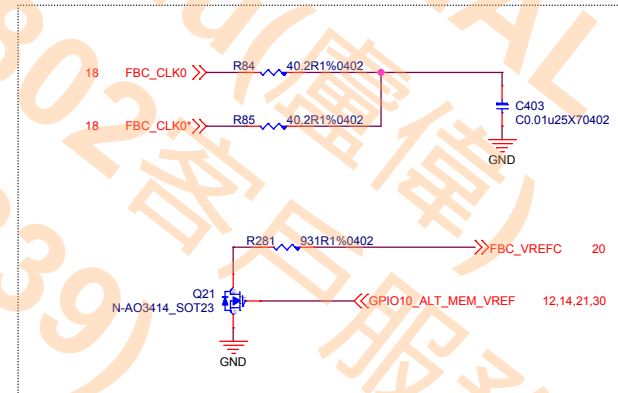
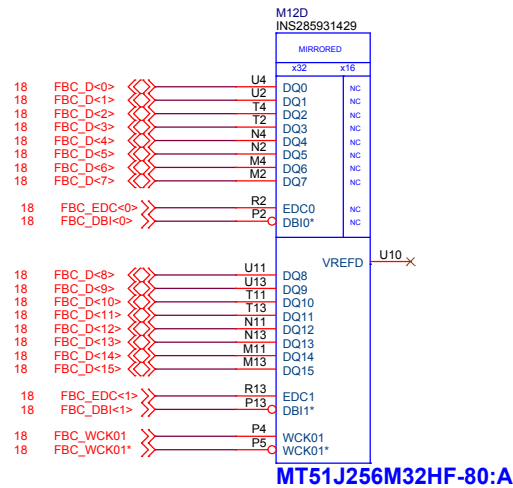
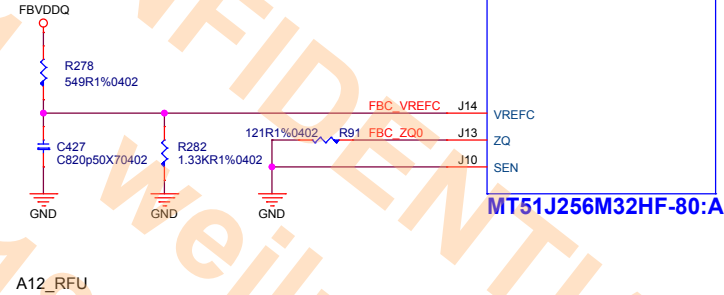
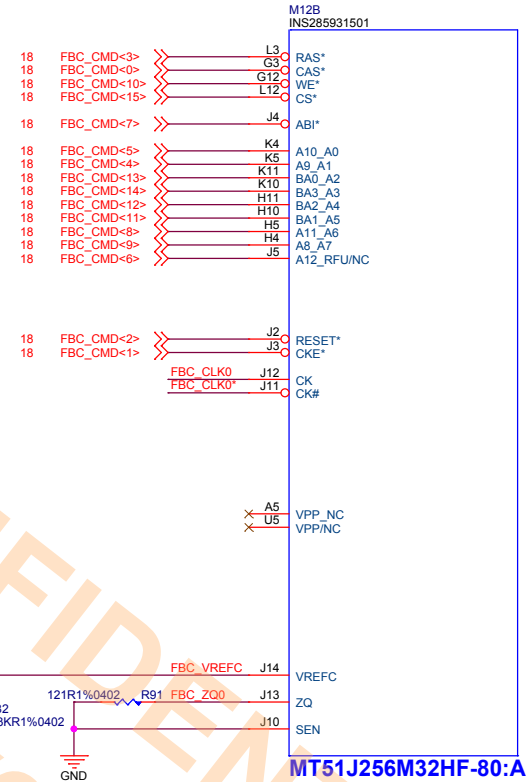
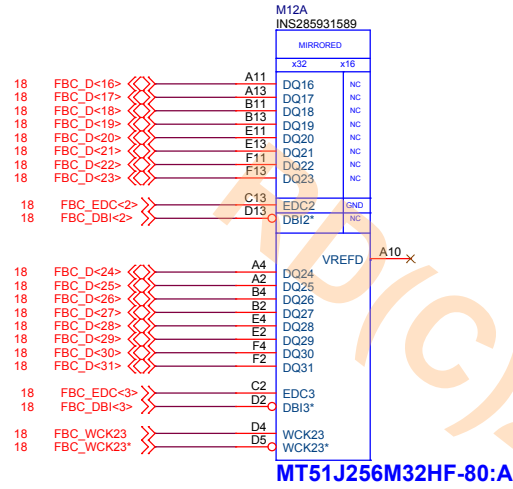
FBD_CLK0	Y8	FBD_CLK0	21
FBD_CLK1	Y7	FBD_CLK0*	21
FBD_CLK1*	R8	FBD_CLK1	22
FBD_CLK1*	R7	FBD_CLK1*	22

FBD_WCK01	AJ8	FBD_WCK01	21
FBD_WCK01*	AJ7	FBD_WCK01#	21
FBD_WCKB01	AG8		
FBD_WCKB01*	AG9		
FBD_WCK23	AD8	FBD_WCK23	21
FBD_WCK23*	AD9	FBD_WCK23#	21
FBD_WCK323	AG7		
FBD_WCK323*	AC8		
FBD_WCK45	J6	FBD_WCK45	22
FBD_WCK45*	J7	FBD_WCK45#	22
FBD_WCKB45	H7		
FBD_WCKB45*	H7		
FBD_WCKB67	P8		
FBD_WCK67	P7	FBD_WCK67	22
FBD_WCKB67*	M7	FBD_WCK67#	22
FBD_WCKB67	M8		

DGPU_GDDR5 FrameBuffer C0

GDD5 Command Mapping GB4-256

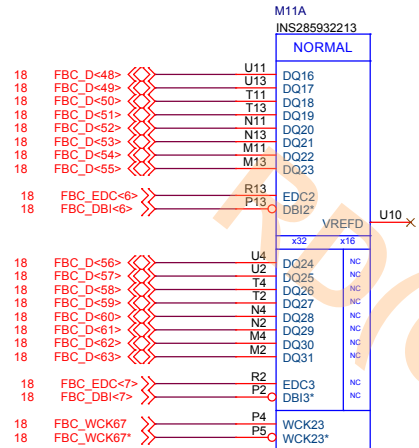
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CAS*
CMD1	CMD17	CKE*
CMD2	CMD18	RST*
CMD3	CMD19	RAS*
CMD4	CMD20	A1 A9
CMD5	CMD21	A0 A10
CMD6	CMD22	A12 RFU
CMD7	CMD23	ABI*
CMD8	CMD24	A6 A11
CMD9	CMD25	A7 A8
CMD10	CMD26	WE*
CMD11	CMD27	A5 BA1
CMD12	CMD28	A4 BA2
CMD13	CMD29	A2 BA0
CMD14	CMD30	A3 BA3
CMD15	CMD31	CS*



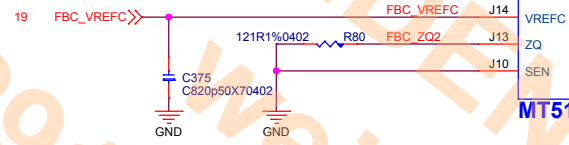
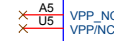
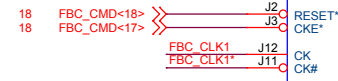
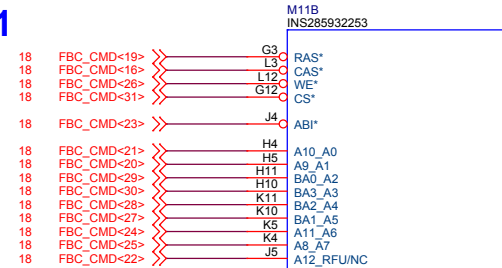
DGPU_GDDR5 FrameBuffer C1

GDD5 Command Mapping GB4-256

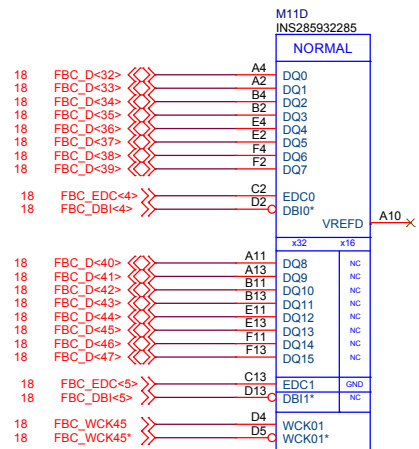
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CAS*
CMD1	CMD17	CKE*
CMD2	CMD18	RST*
CMD3	CMD19	RAS*
CMD4	CMD20	A1 A9
CMD5	CMD21	A0 A10
CMD6	CMD22	A12 RFU
CMD7	CMD23	ABI*
CMD8	CMD24	A6 A11
CMD9	CMD25	A7 A8
CMD10	CMD26	WE*
CMD11	CMD27	A5 BA1
CMD12	CMD28	A4 BA2
CMD13	CMD29	A2 BA0
CMD14	CMD30	A3 BA3
CMD15	CMD31	CS*



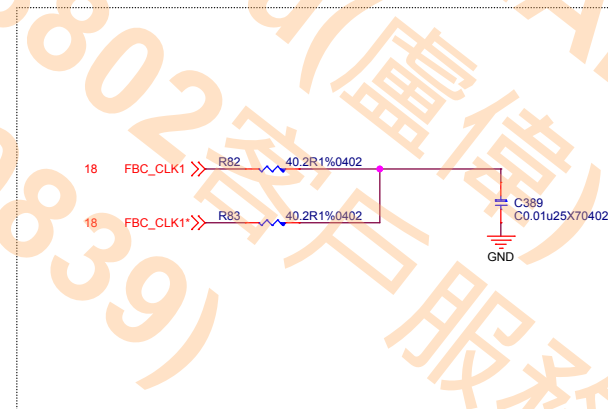
MT51J256M32HF-80:A



MT51J256M32HF-80:A



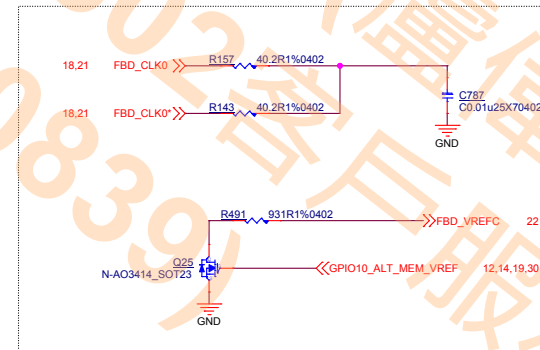
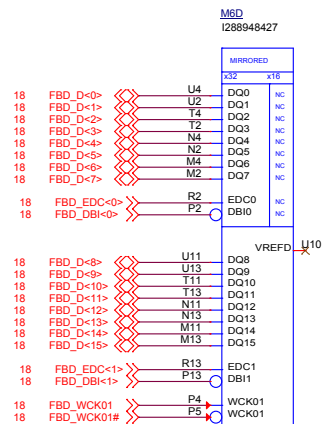
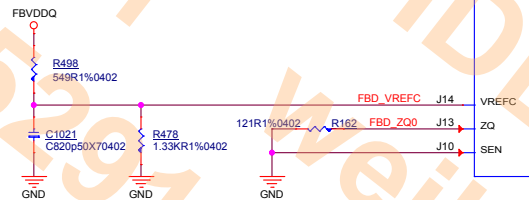
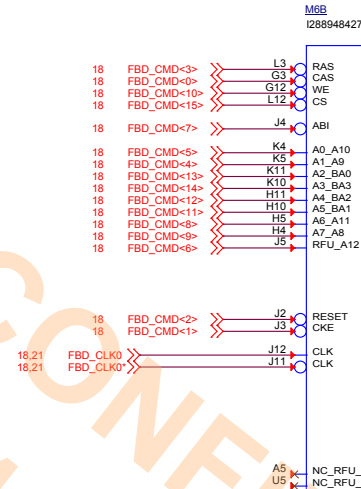
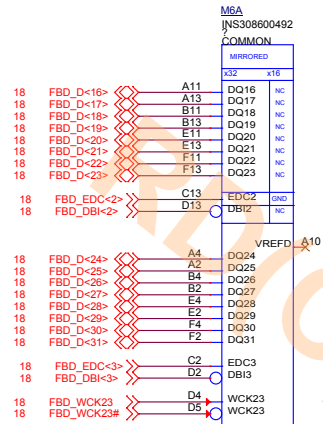
MT51J256M32HF-80:A



DGPU_GDDR5 FrameBuffer D0

GDD5 Command Mapping GB4-256

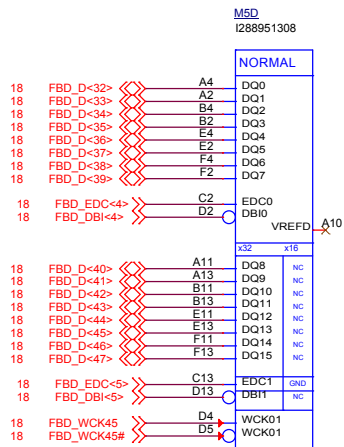
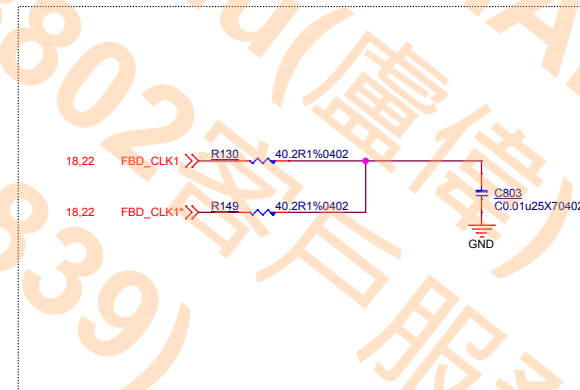
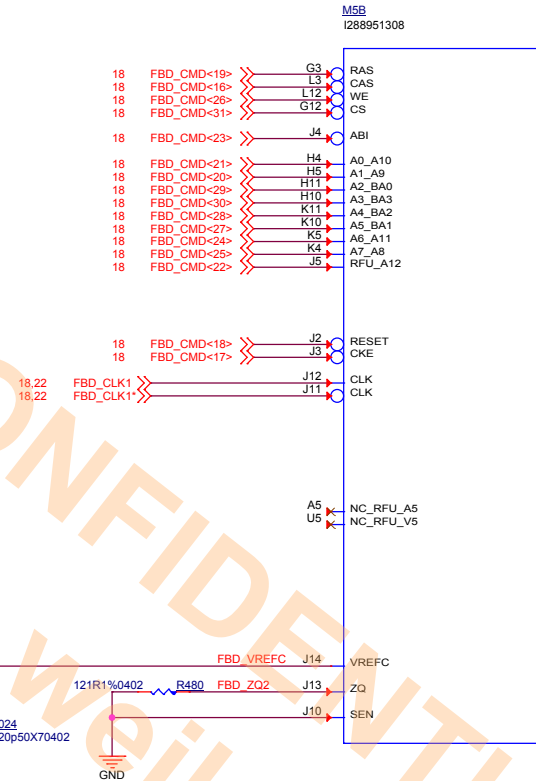
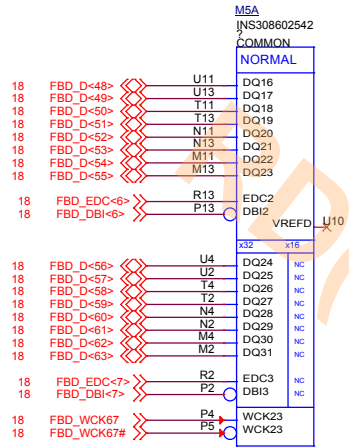
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CAS*
CMD1	CMD17	CKE*
CMD2	CMD18	RST*
CMD3	CMD19	RAS*
CMD4	CMD20	A1 A9
CMD5	CMD21	A0 A10
CMD6	CMD22	A12 RFU
CMD7	CMD23	ABI*
CMD8	CMD24	A6 A11
CMD9	CMD25	A7 A8
CMD10	CMD26	WE*
CMD11	CMD27	A5 BA1
CMD12	CMD28	A4 BA2
CMD13	CMD29	A2 BA0
CMD14	CMD30	A3 BA3
CMD15	CMD31	CS*



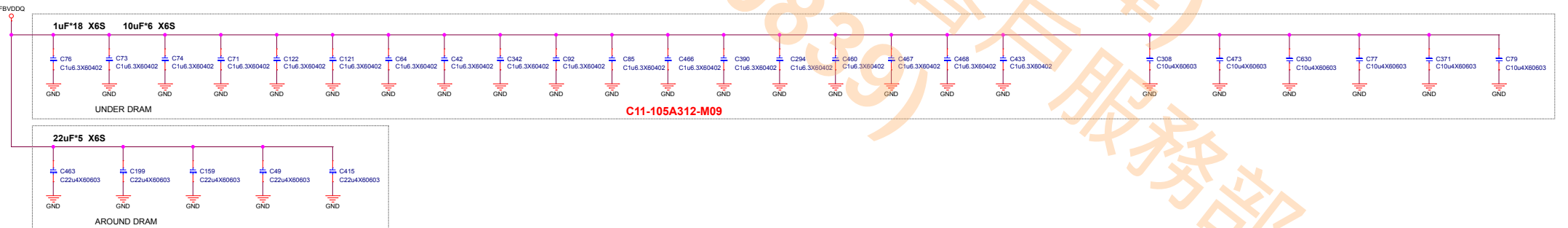
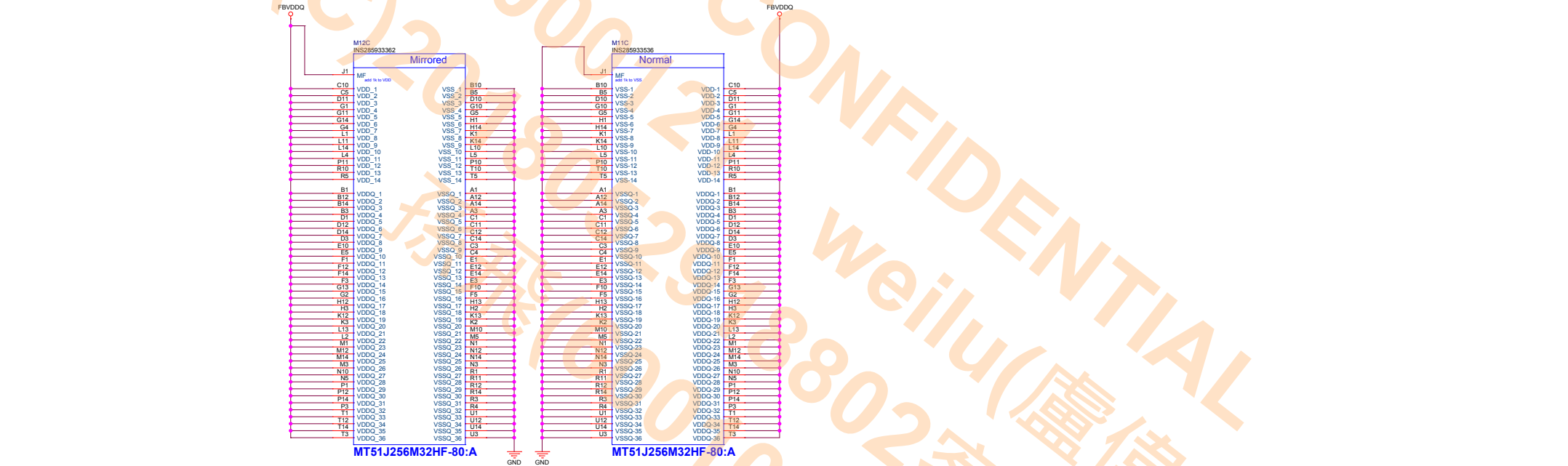
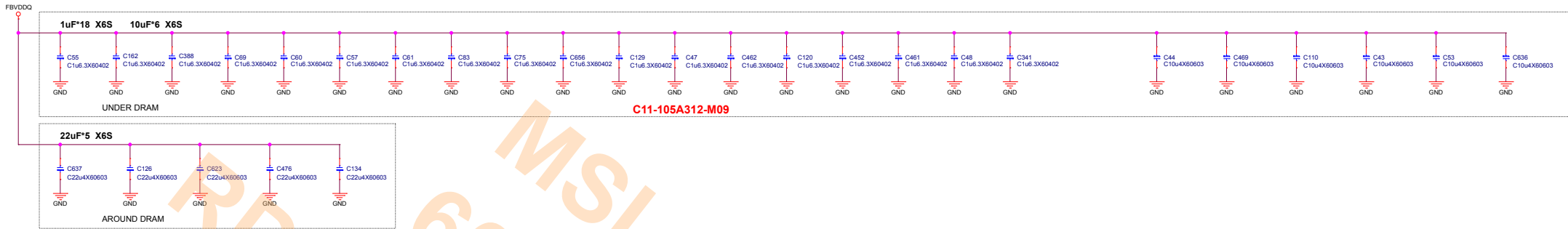
DGPU_GDDR5 FrameBuffer D1

GDD5 Command Mapping GB4-256

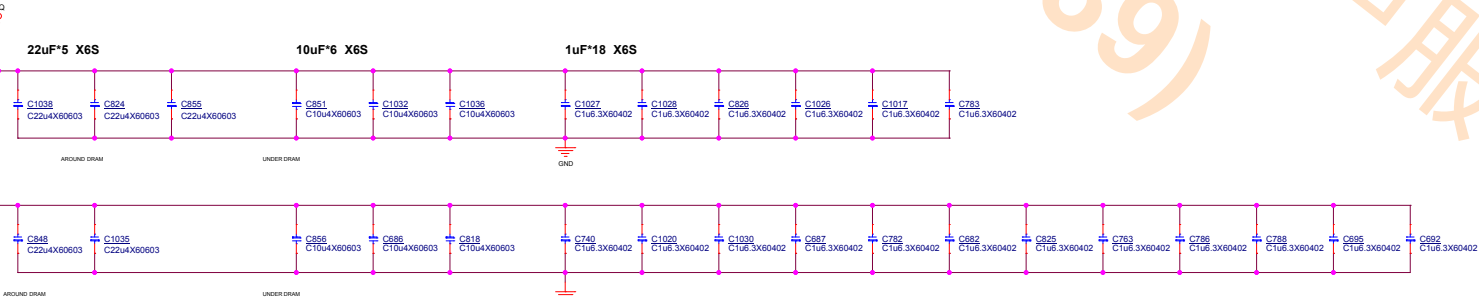
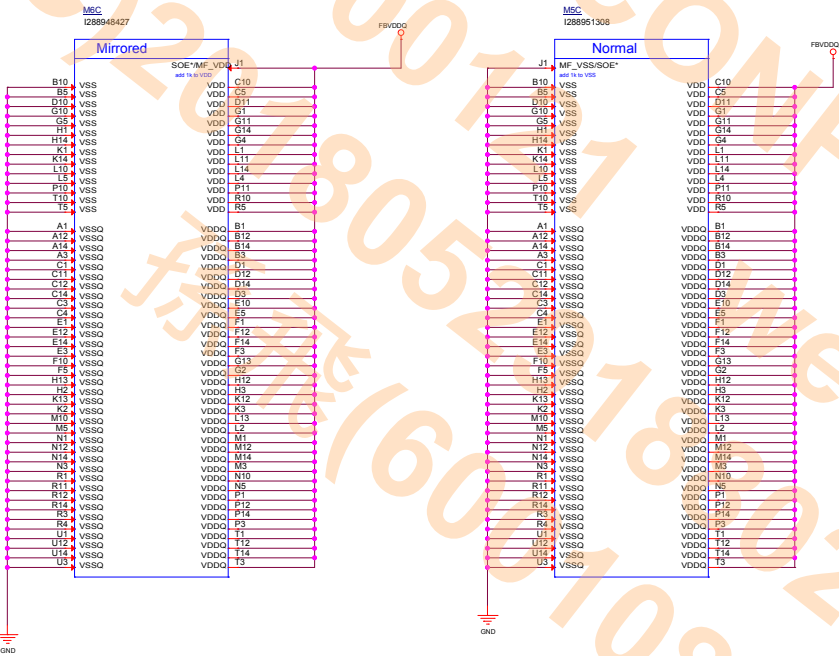
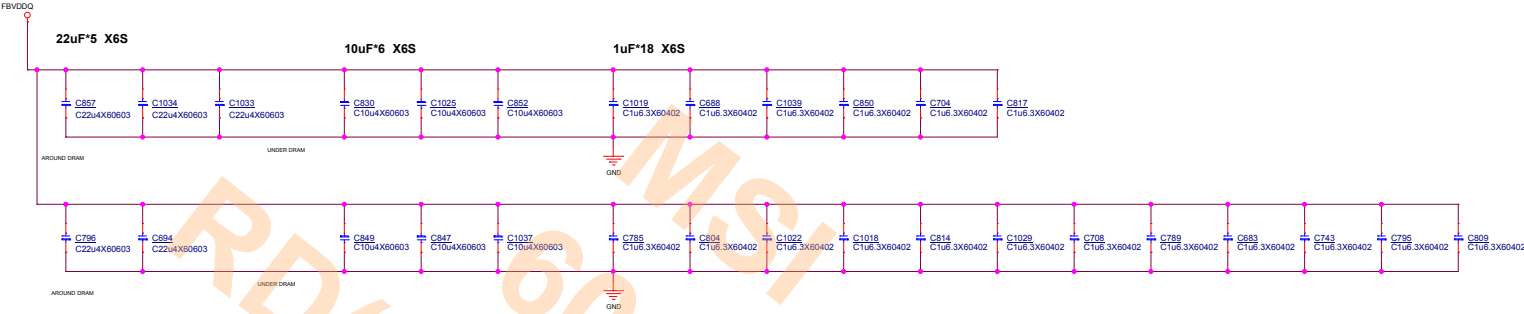
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CAS*
CMD1	CMD17	CKE*
CMD2	CMD18	RST*
CMD3	CMD19	RAS*
CMD4	CMD20	A1 A9
CMD5	CMD21	A0 A10
CMD6	CMD22	A12 RFU
CMD7	CMD23	ABI*
CMD8	CMD24	A6 A11
CMD9	CMD25	A7 A8
CMD10	CMD26	WE*
CMD11	CMD27	A5 BA1
CMD12	CMD28	A4 BA2
CMD13	CMD29	A2 BA0
CMD14	CMD30	A3 BA3
CMD15	CMD31	CS*



Frame Buffer Partition C Decoupling



Frame Buffer Partition D Decoupling

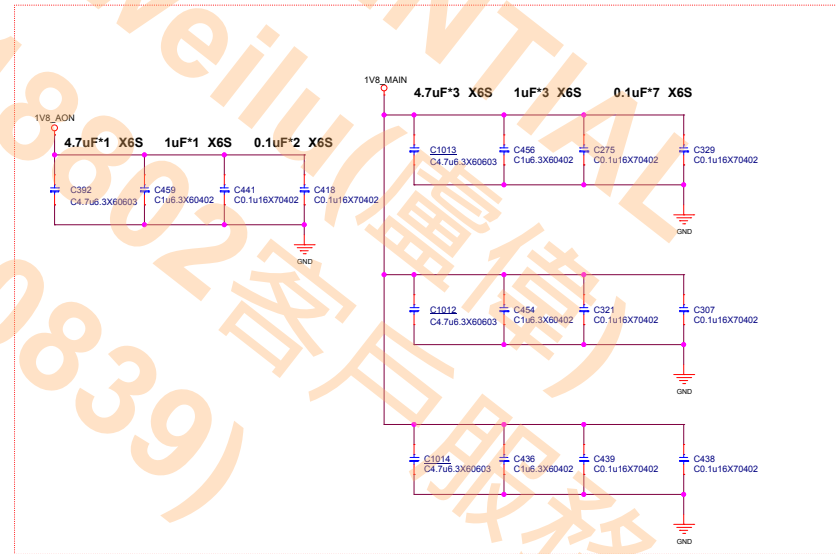
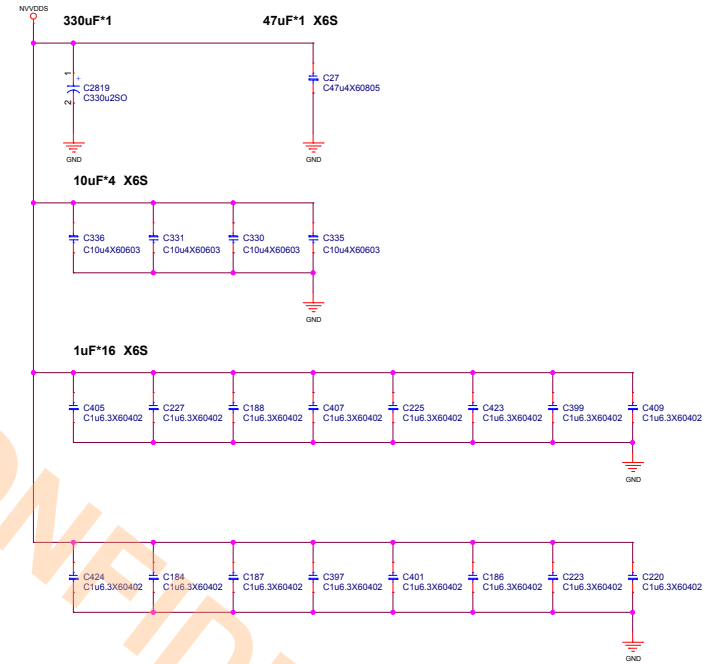


GPU DECOUPLING A

NVDD



VDDS



GPU DECOUPLING B

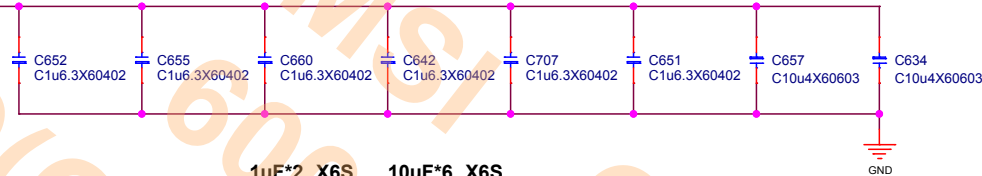
FBVDDQ

FBVDDQ

Partition A

1uF*2 X6S

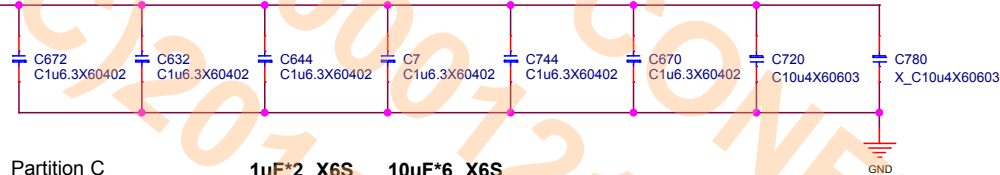
10uF*6 X6S



Partition B

1uF*2 X6S

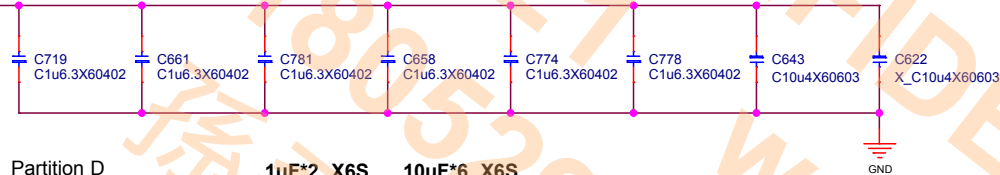
10uF*6 X6S



Partition C

1uF*2 X6S

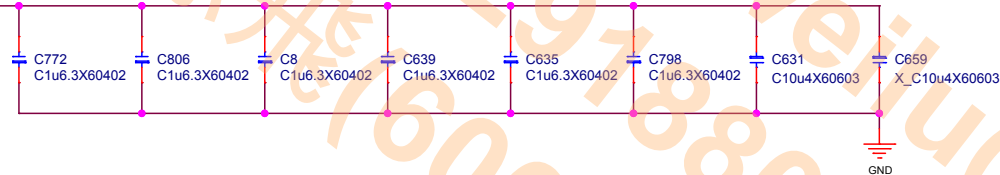
10uF*6 X6S



Partition D

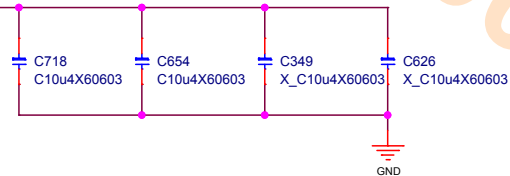
1uF*2 X6S

10uF*6 X6S

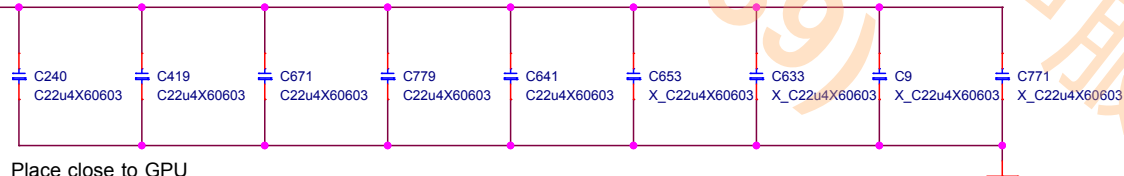


Place close to GPU


10uF*4 X6S



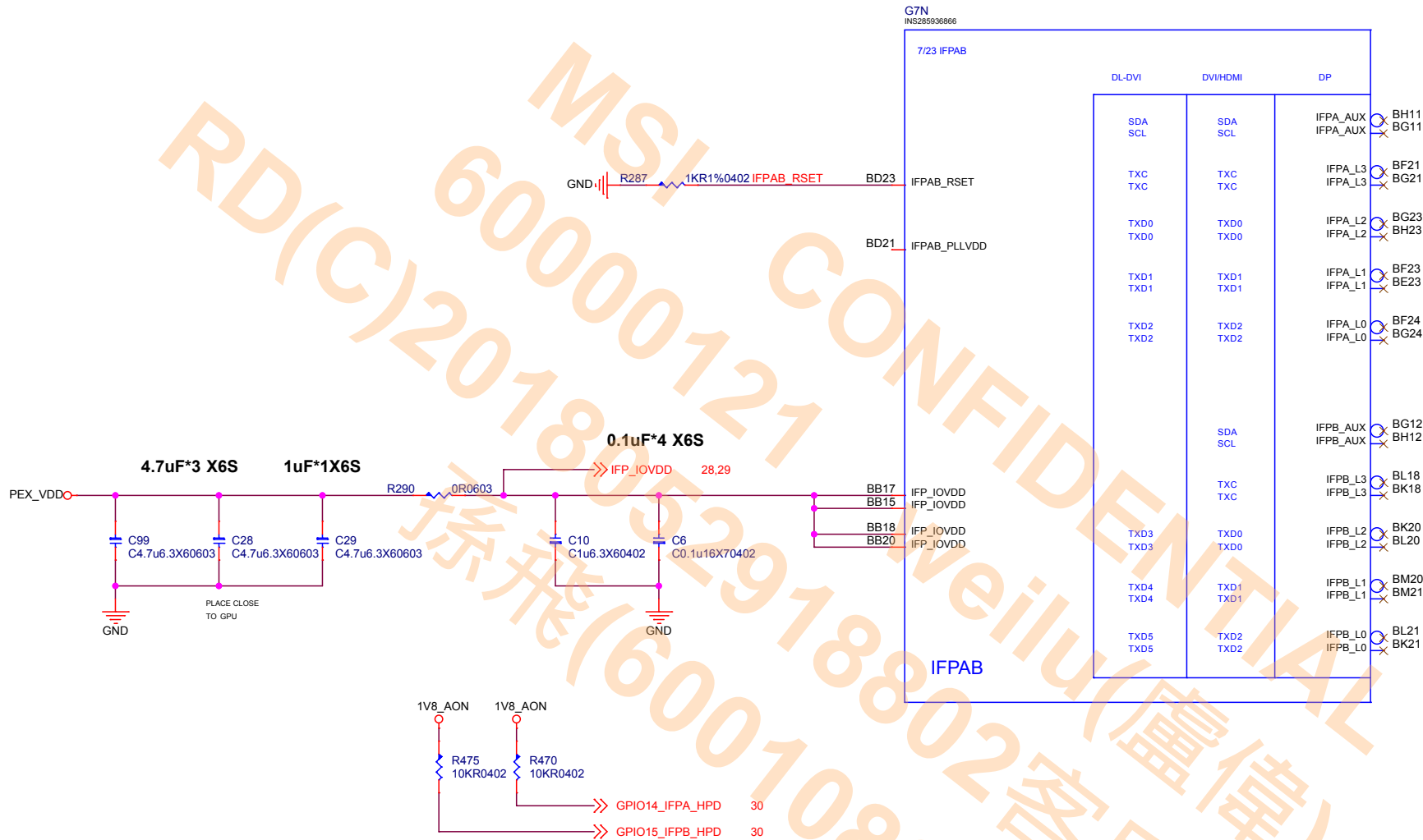
22uF*9 X6S



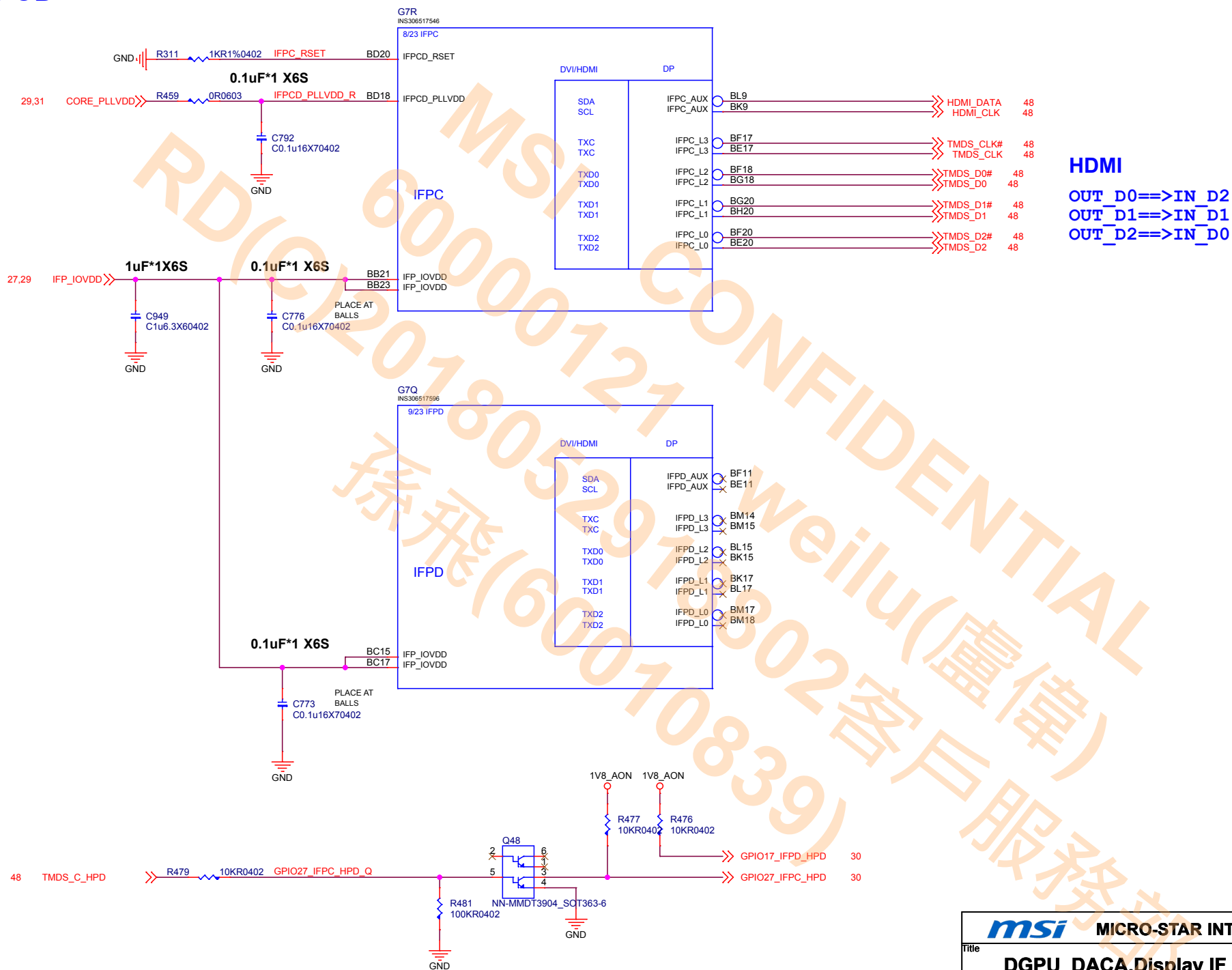
Place close to GPU

		MICRO-STAR INT'L CO.,LTD.	
Title		DGPU GPU DECOUPLING B	
Size	Document Number	Rev	
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IFPCD



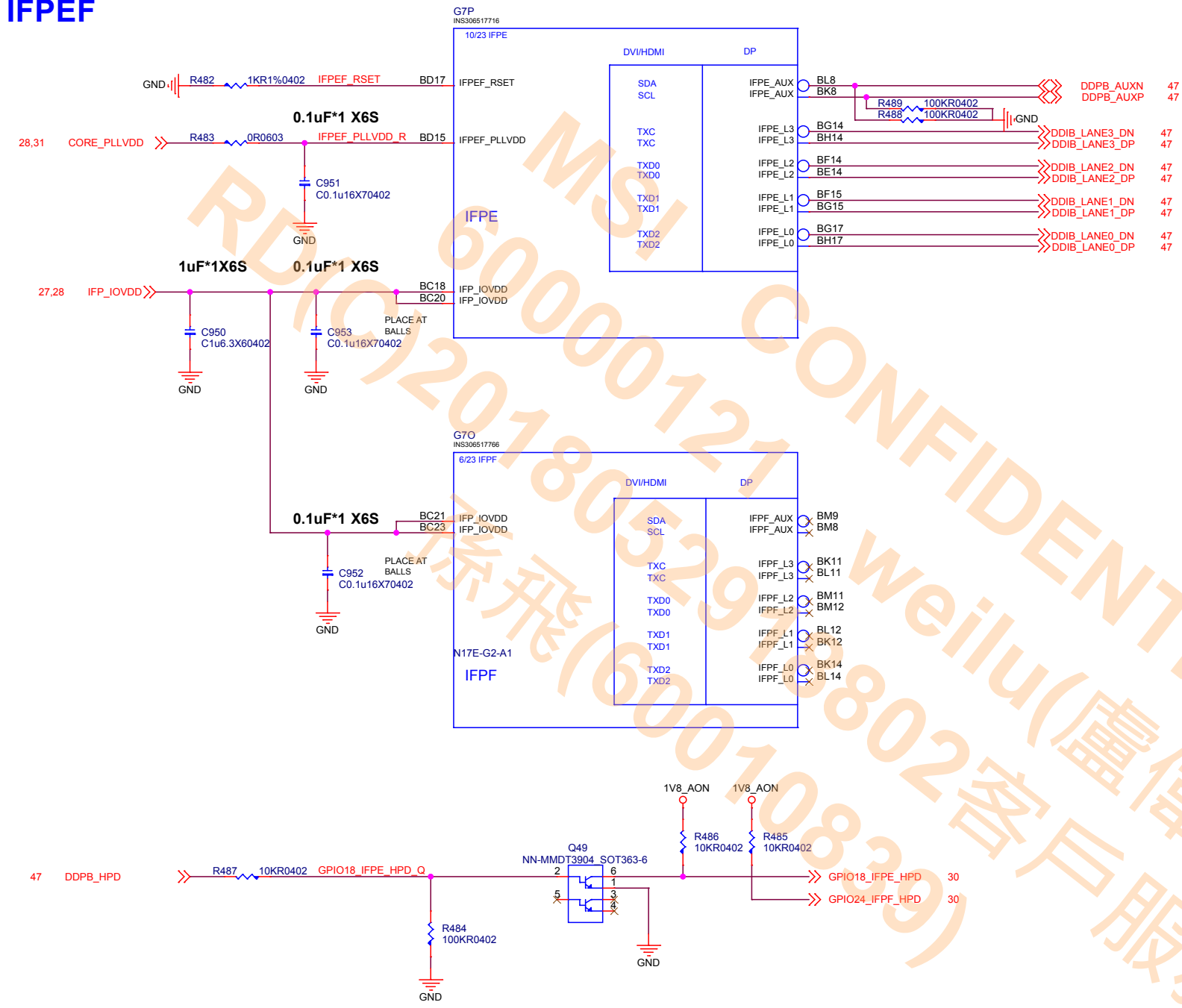
IFPCD



HDMI

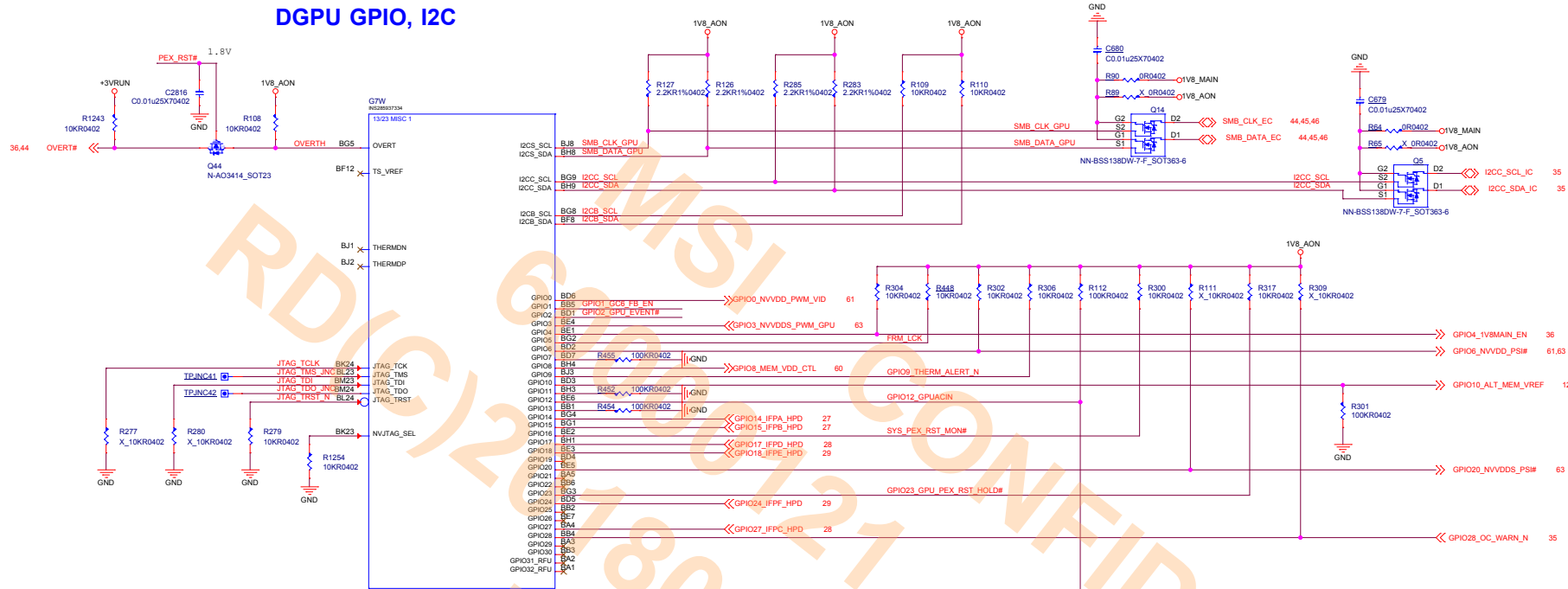
```
OUT_D0==>IN_D2
OUT_D1==>IN_D1
OUT_D2==>IN_D0
```

IFPEF

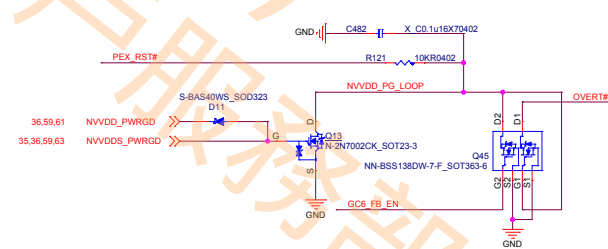
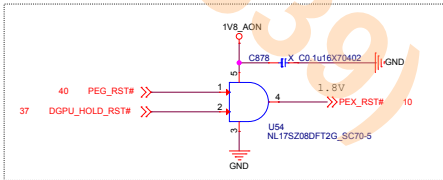
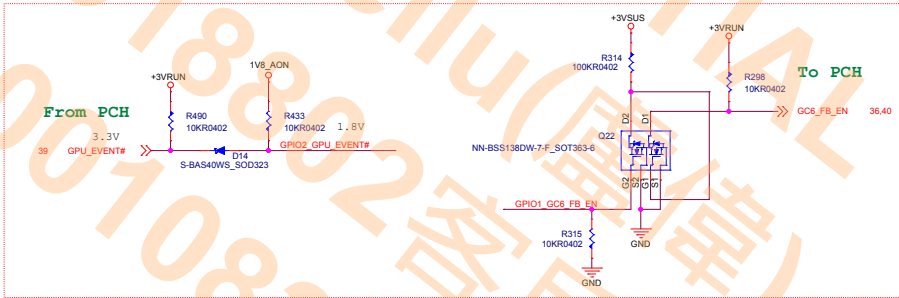


DP

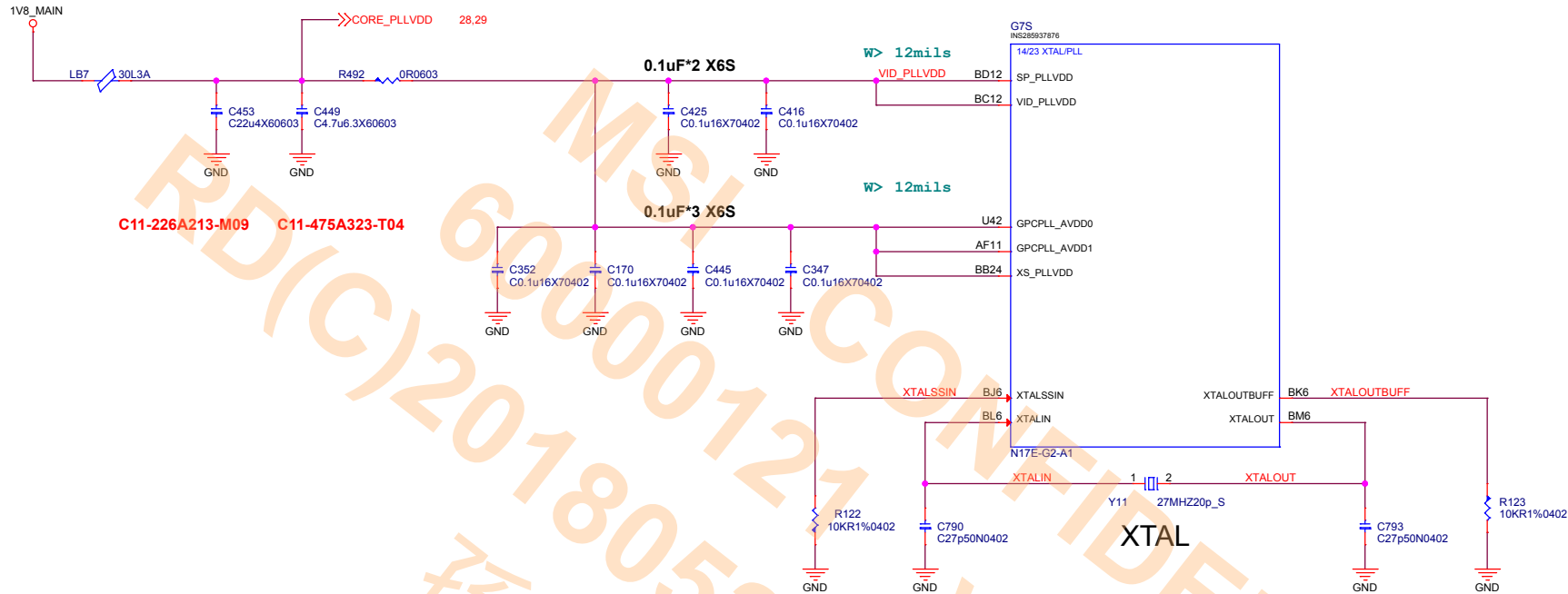
DGPU GPIO, I2C



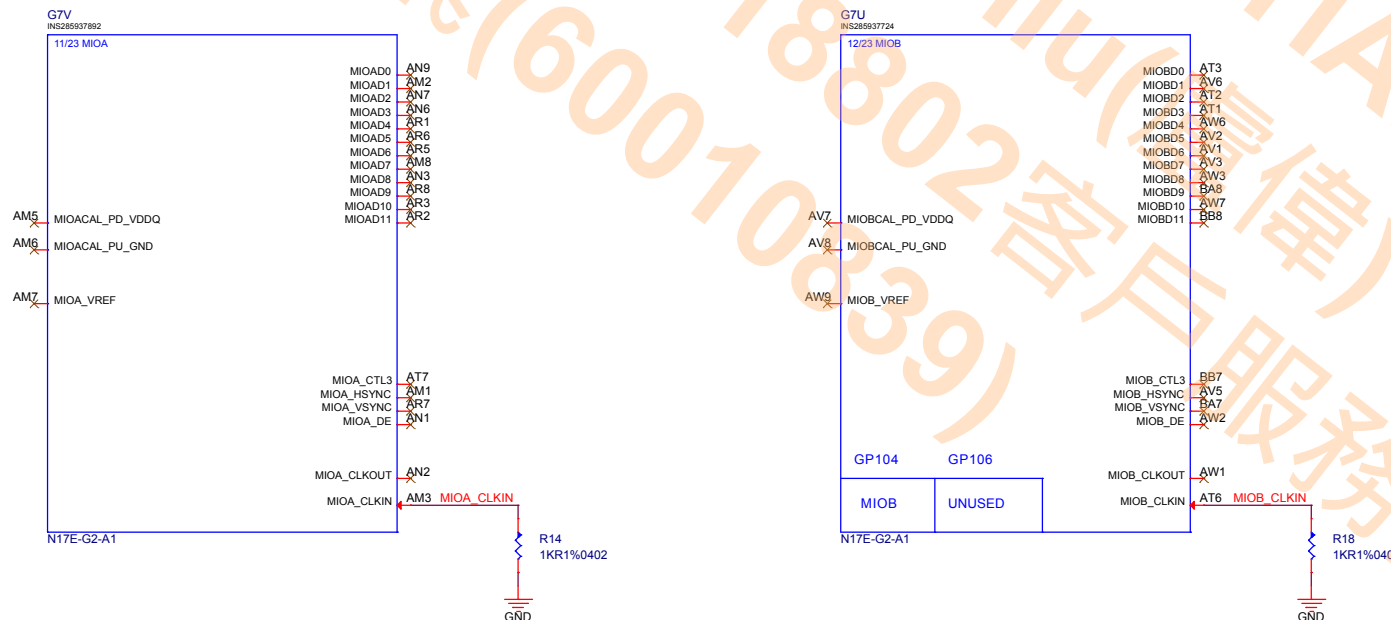
Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	PWM Output to Control NVVD	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8_AON
GPIO3	NVVDDS_PWM	O	PWM output to control the NVVDDS power supply	0 to 1V8 PWM output
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	10K pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Fram Lock	10K pull-up to 1V8_AON
GPIO6	NVVDD_PSI	O	Phase shedding	10K pull-up to 1V8_AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FRM/LCK power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	10K pull-up to 1V8_AON
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	10K pull-up to 1V8_AON
GPIO16	SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 1V8_AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	10K pull-up to 1V8_AON
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	10K pull-up to 1V8_AON
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	NVVDDS_PSI	O	Phase shedding	10K pull-up to 1V8_AON
GPIO21	SLI_RASTER_SYNC	I	SLI Raster Sync	100K pull-down
GPIO22	SLI_SWAP_DRY	I	SLI Swap Ready	
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIe self-reset control	10K pull-up to 1V8_AON
GPIO24	HPD_F	I	Hot Plug Detect for IFPDE	10K pull-up to 1V8_AON
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	10K pull-up to 1V8_AON
GPIO28	OC_WARN	I	Over current throttling	10K pull-up to 1V8_AON
GPIO29	EDPC_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	RESERVED			



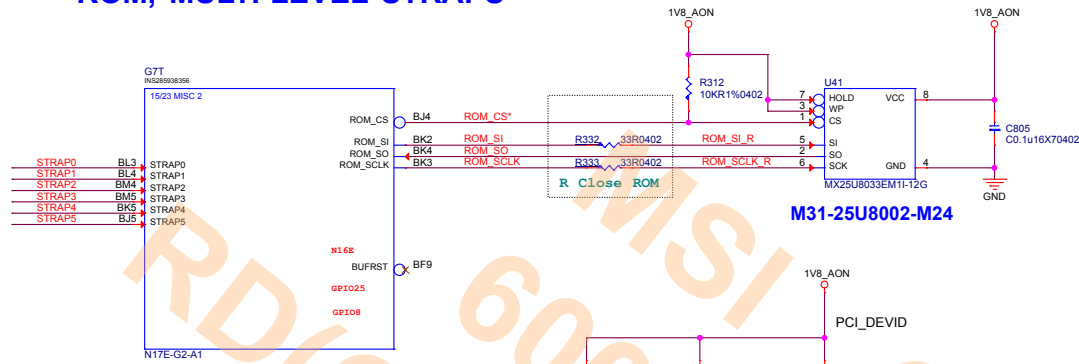
DGPU MIO & XTAL



Multi-use IO(MIO) Interface



ROM, MULTI-LEVEL STRAPS



ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED3	SOR_EXPOSED2	SOR_EXPOSED1	SOR_EXPOSED0
L	L	L	1:ENABLE	1:ENABLE	1:ENABLE	1:ENABLE
L	L	H	1:ENABLE	1:ENABLE	1:ENABLE	0:DISABLE
L	H	L	1:ENABLE	1:ENABLE	0:DISABLE	1:ENABLE
L	H	H	1:ENABLE	1:ENABLE	0:DISABLE	0:DISABLE
H	H	H	1:ENABLE	0:DISABLE	0:DISABLE	0:DISABLE
H	H	M	0:DISABLE	0:DISABLE	0:DISABLE	0:DISABLE

STRAP 5	STRAP 4	STRAP 3	
L	L	L	Optimus
L	L	H	Discrete
H	L	H	Discrete with Gsync

STRAP 2	STRAP 1	STRAP 0		
L	L	L	0x0	Samsung K4G80325FB-HC25
L	L	H	0x1	Microm MT51J2256M32HF-80:A
L	H	L	0x2	Hynix H5GC8H24MJR-R4C
H	H	L	0x6	Hynix H5GQ4H24AJR-R4C
H	H	H	0x7	Samsung K4G41325FE-HC25

V_BOT1

Samsung
256Mx32bit

☐ M12-8032535-S02
X_K4G80325FB-HC25

V_BOT2

Samsung
128Mx32bit

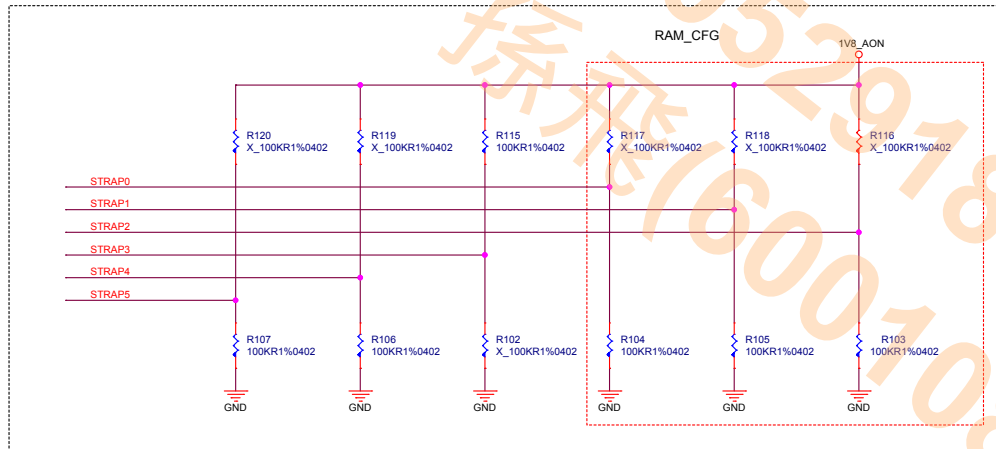
☐ M12-41325D5-S02
X_K4G41325FE-HC25

N17E-G2
(GTX1070)

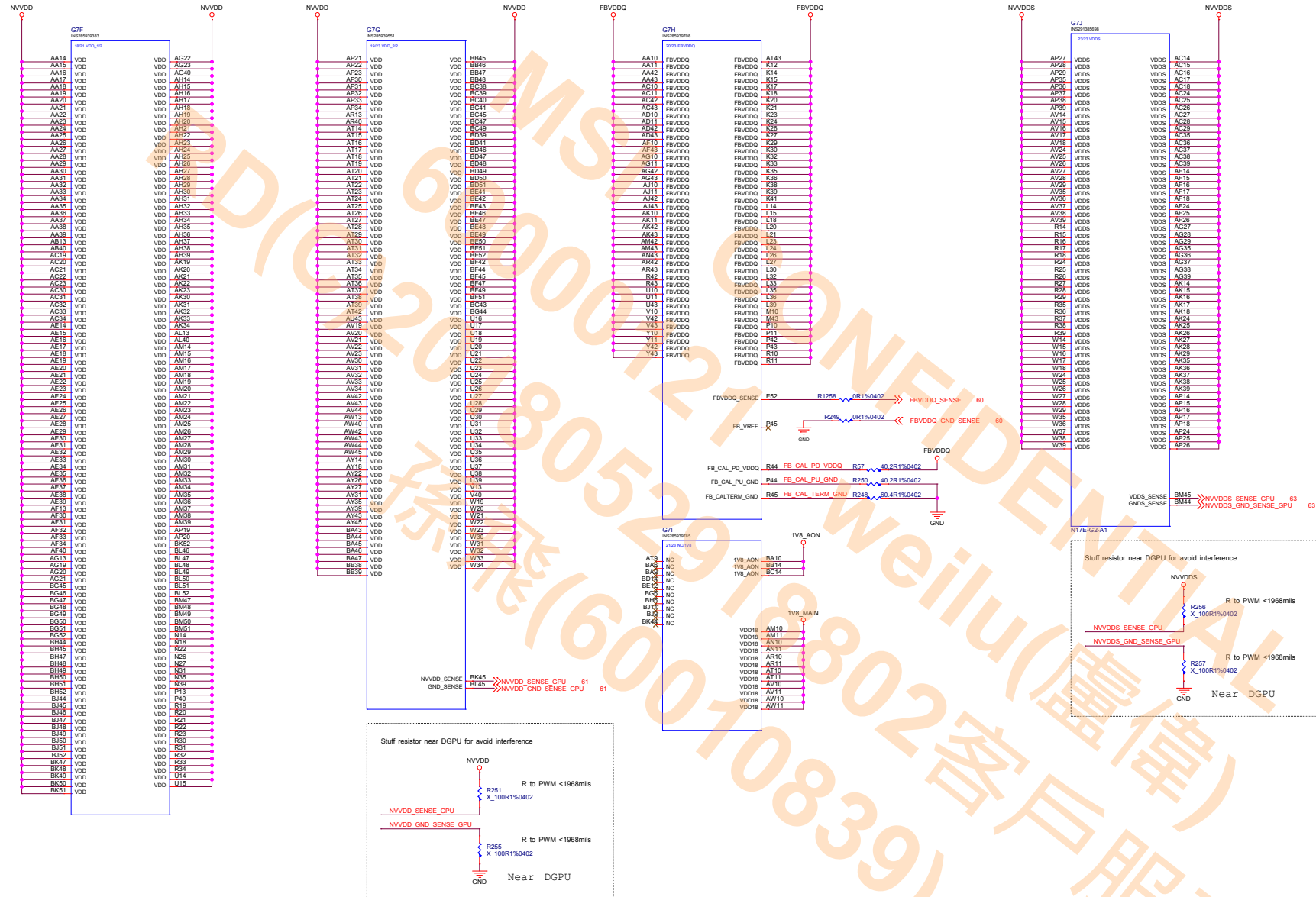
N17E_G2
☐ B03-0N17E05-N08
X_N17E-G2-A1

N17E-G1
(GTX1060)

N17E_G1
☐ B03-0N17E25-N08
X_N17E-G1-A1



GPU NVVDD, FBVDDQ

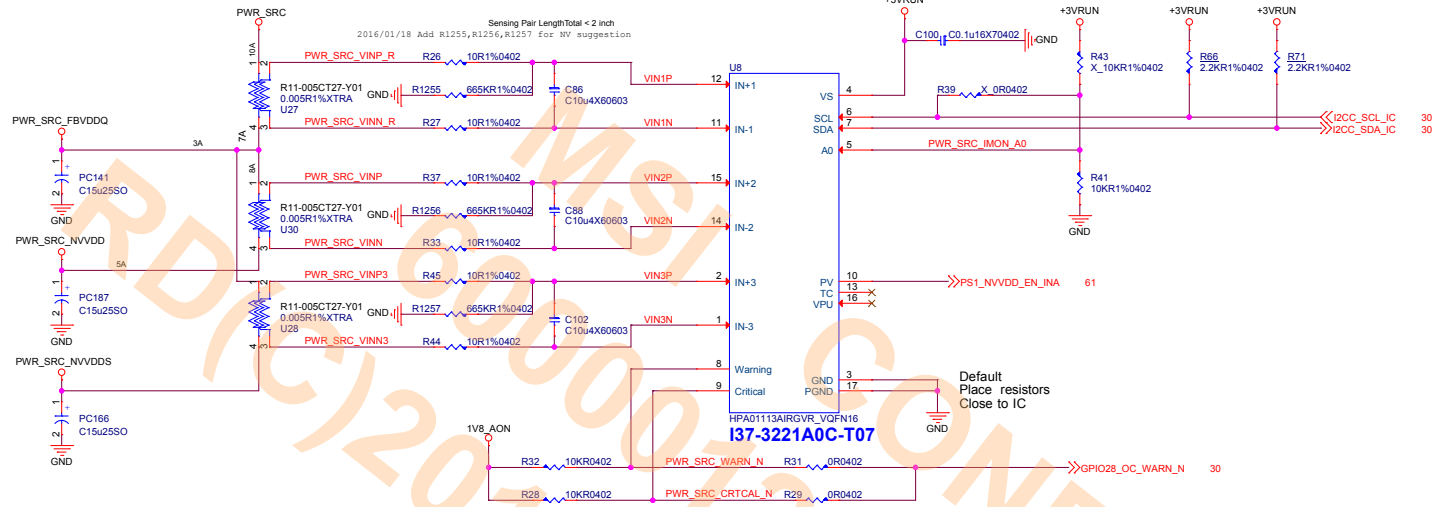


DGPU GND

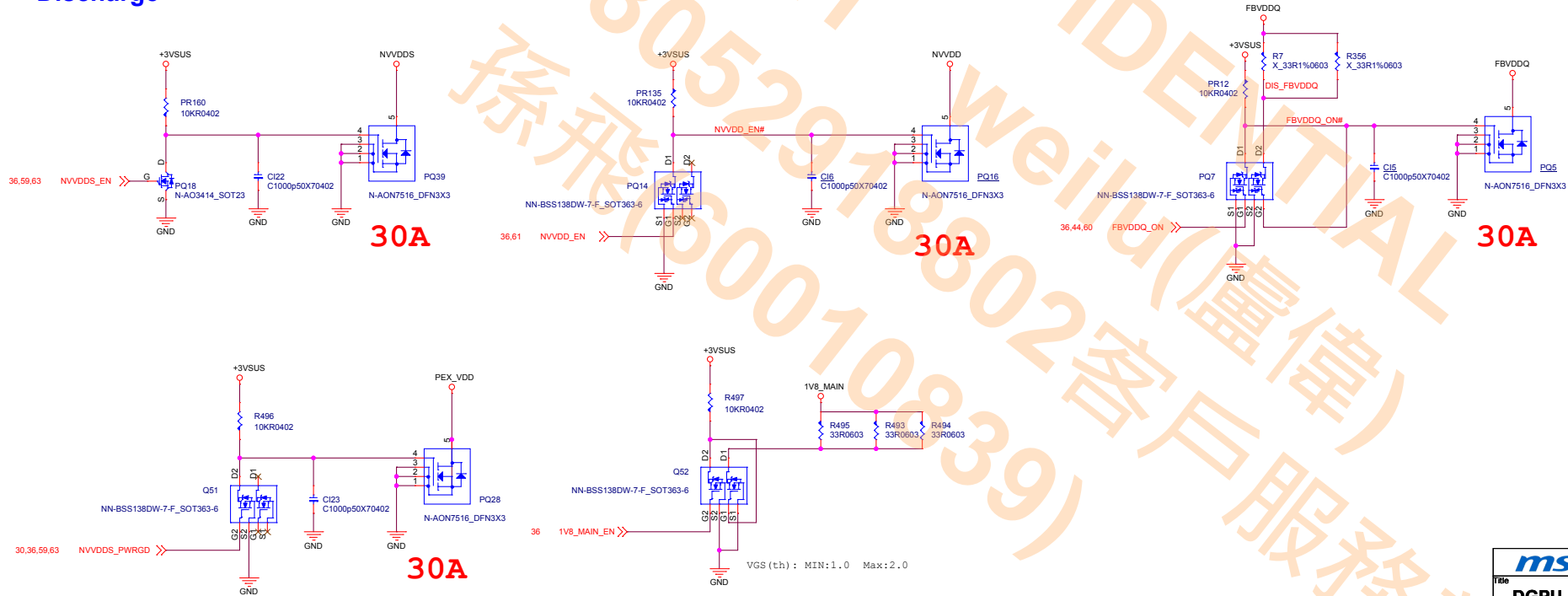


EDP Design Guide:
N17E-G1(90W)
NVVDD : 58A ; Peak 136A
NVVDDS : 28A ; Peak 74A
1.8V : 0.9A
PEX_VDD : 3A
FBVDDQ : 16A

DGPU Power Measurement



Discharge

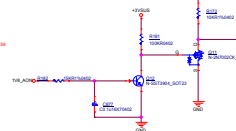


msi MICRO-STAR INT'L CO.,LTD.	
Title DGPU Power Measurement	
Size Document Number	Rev 1.0
MS-16JE	
Date:	Sheet 35 of 75

1V8_AON



1V8_AON POWER GOOD

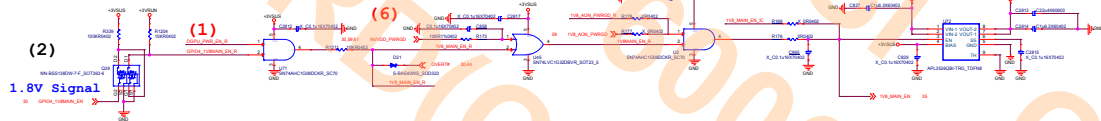


1V8_MAIN POWER GOOD

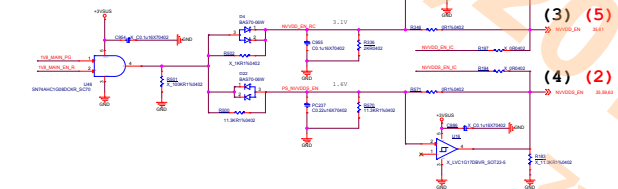


1V8_MAIN

1.8V Signal



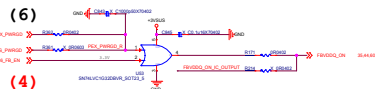
NVVDD/NVDD



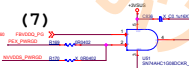
PEX_VDD



FBVDDQ

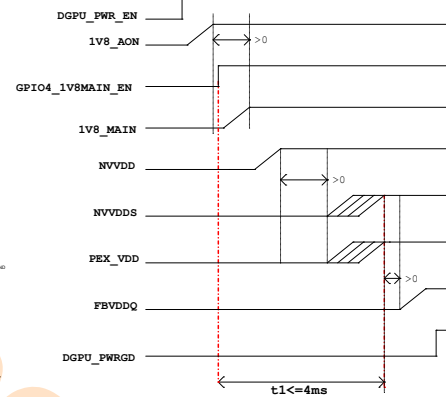


DGPU POWER GOOD



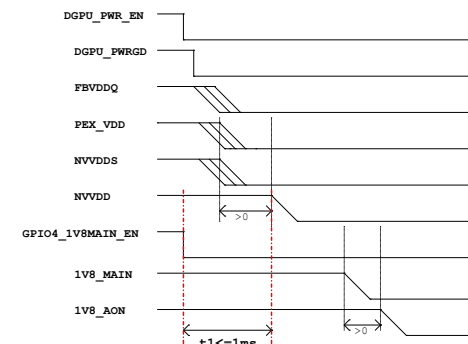
POWER UP Sequence

1V8_AON -> 1V8_MAIN->NV3V3 -> NVVDD -> NVVDD / PEX_VDD -> FBVDDQ

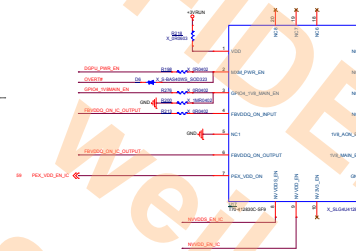


POWER Down Sequence

NVVDD/PEX_VDD/FBVDDQ ->NVVDD/NV3V3->1V8_MAIN-> 1V8_AON



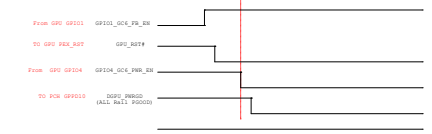
SLG4U41283 Power Sequence Control IC



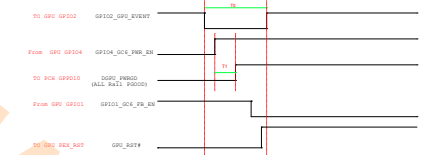
Pin2: MUX PWR_EN is 3.3V
Pin3: GPIO4_GC6_PWR_EN is 1.8V
Pin4: FBVDDQ_ON INPUT 3.3V
Pin6: FBVDDQ_ON OUTPUT 3.3V
Pin7: PEX_VDD_EN IC 3.3V
Pin9: NVVDD_EN IC 3.3V
Pin12: 1V8_MAIN_EN IC 3.3V
Pin13: 1V8_AON_EN IC 3.3V
(Pin13: PULL DOWN 100K)

INPUT
INPUT
OUTPUT
OUTPUT
OUTPUT
OUTPUT
OUTPUT
OUTPUT

GC6 2.1 ENTRY SEQUENCE



GC6 2.1 EXIT SEQUENCE



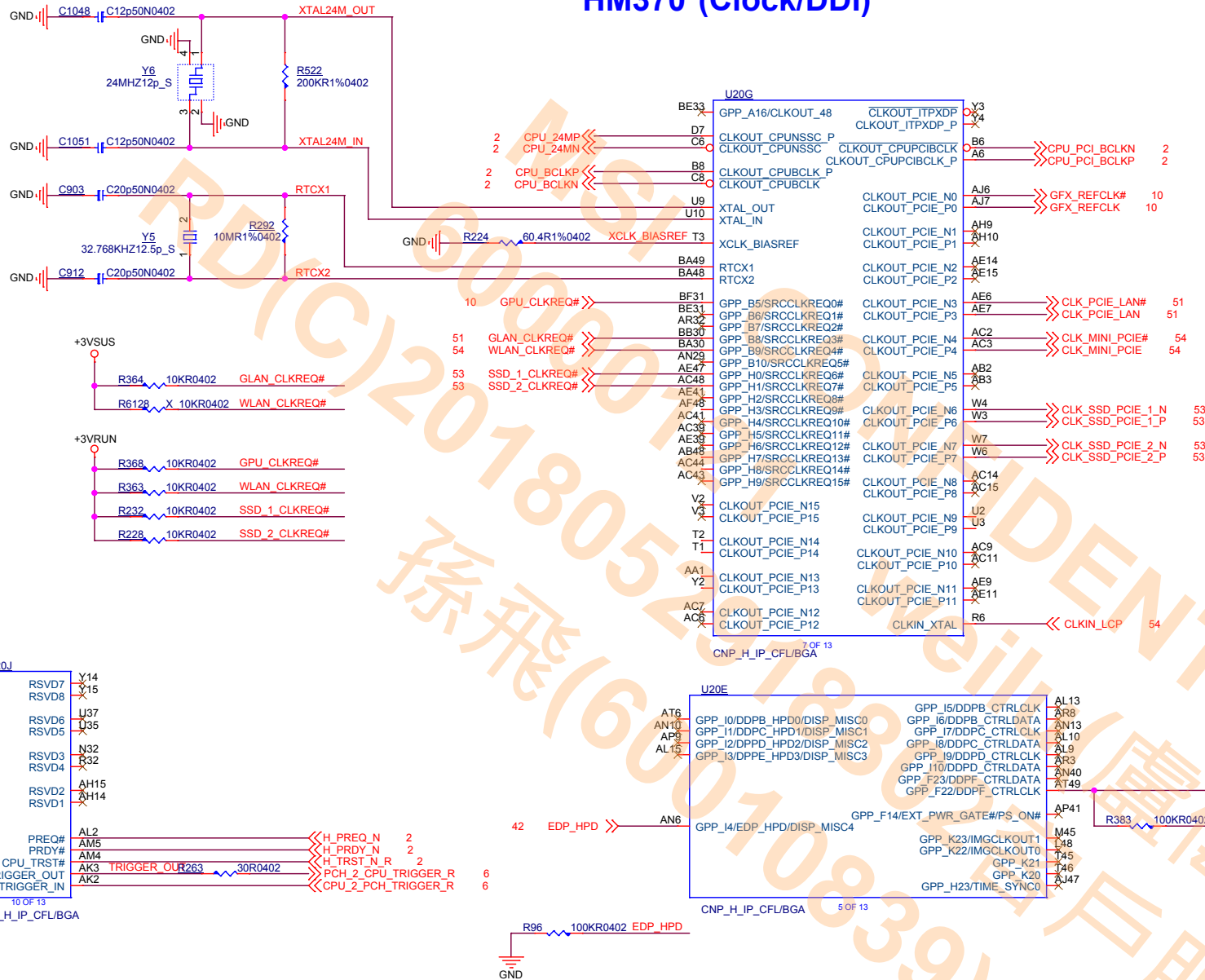
GC6 2.1 TIMING

	Min	Max	Unit	Description
t1	0.001	N/A	ms	GPU EVENT# assertion
t1	0.04	4	ms	3V3 MAIN EN assertion to all power rails up and stable

NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

HM370 (Clock/DDI)



Functional Strap Definitions

DDPB_CTRLDATA / GPP_I6

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPC_CTRLDATA / GPP_I8

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPD_CTRLDATA / GPP_I10

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

GPP_F23

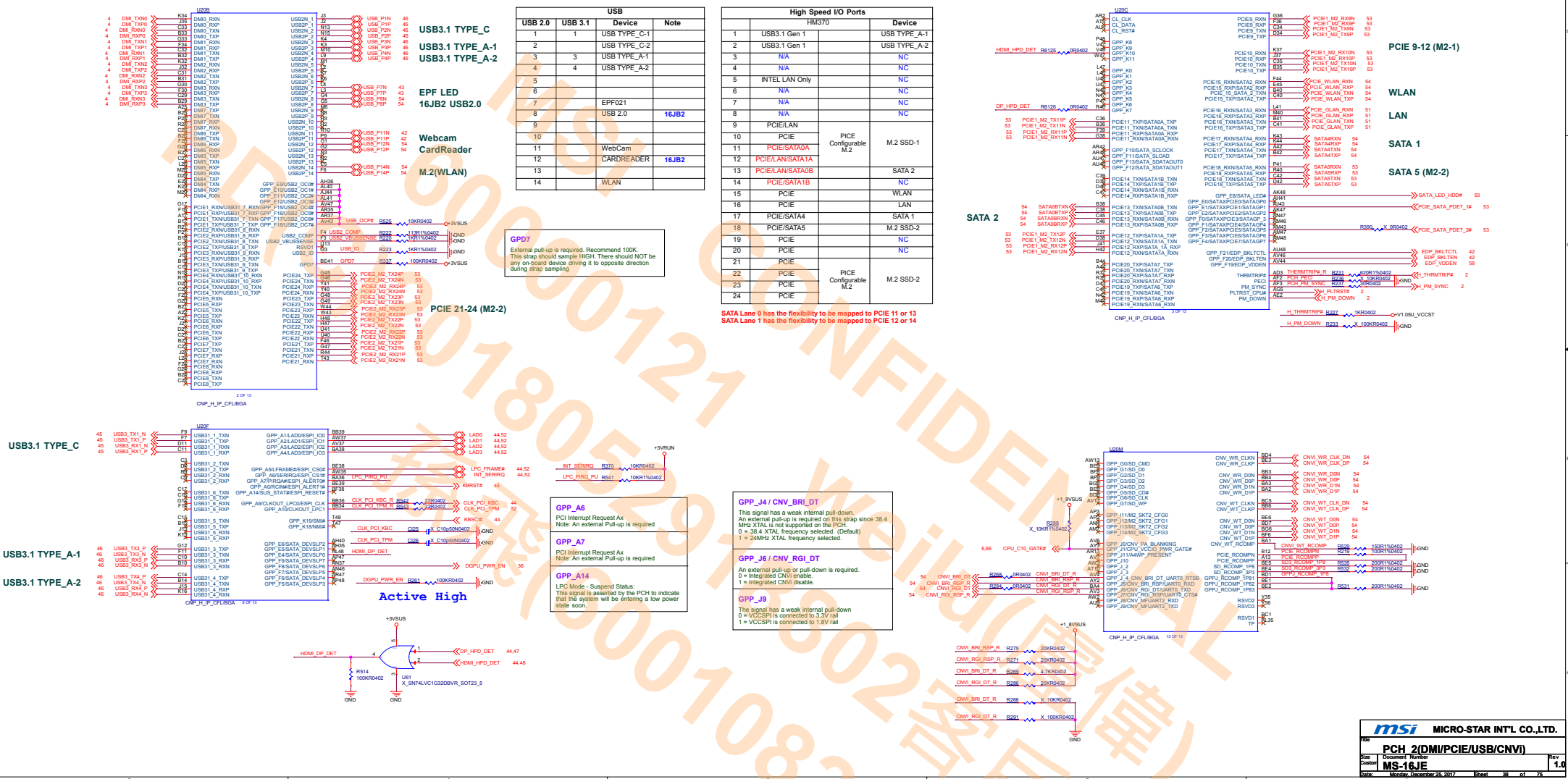
This signal has a weak internal pull-down.
0 = Port F is not detected. (Default)
1 = Port F is detected.



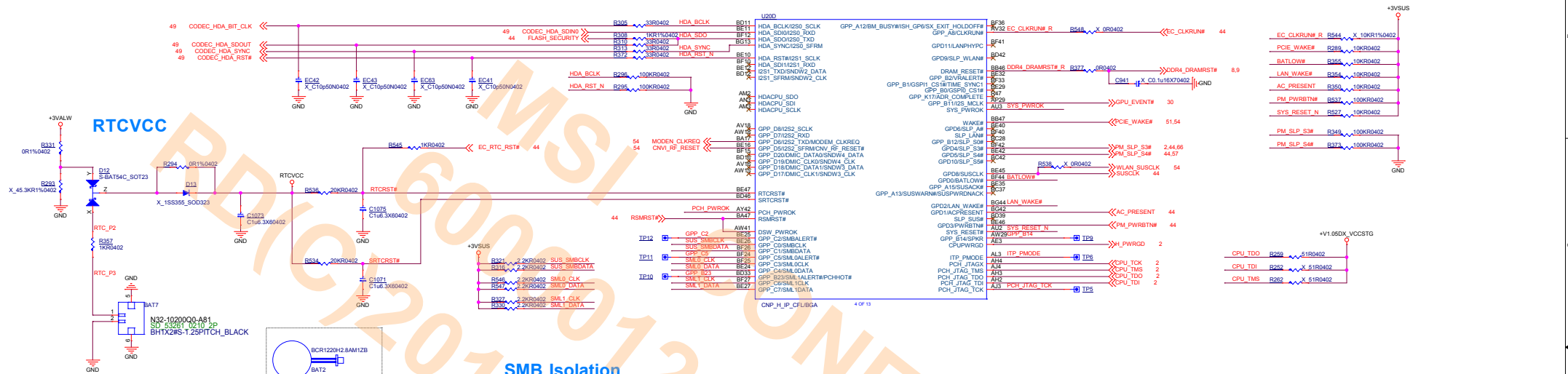
MICRO-STAR INT'L CO.,LTD.

Title			
PCH 1(CLK/DDI)			
Size B	Document Number		Rev
	MS-16JE		1.0
Date:	Monday, December 25, 2017	Sheet	37 of 75

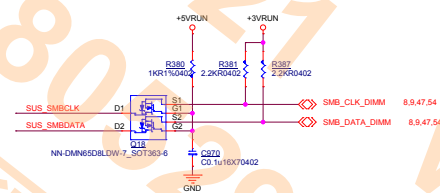
HM370 (DMI/PCIE/USB/CNVi)



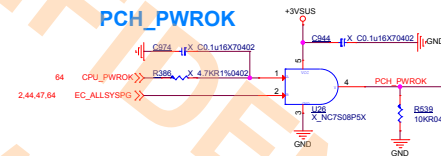
HM370 (HDA/RTC/SMBUS)



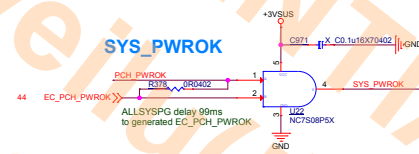
SMB Isolation



PCH_PWROK



SYS_PWROK



Functional Strap Definitions

HDA_SDO / I2S0_TXD

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).

SMBALERT# / GPP_C2

This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

SML0ALERT# / GPP_C5

This signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

SML1ALERT# / PCHHOT# / GPP_B23

This signal has an internal pull-down.
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB

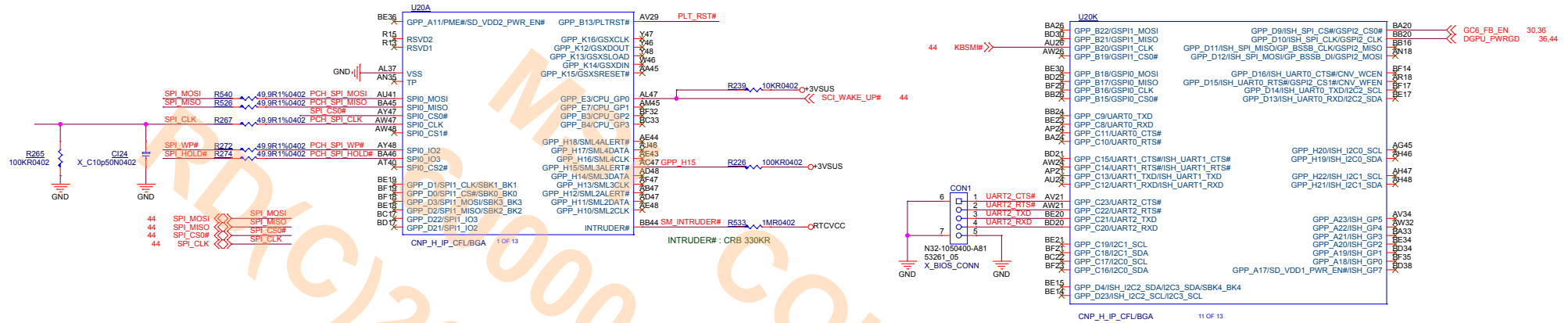
SPKR / GPP_B14

The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)
1 = Enable Top Swap mode.

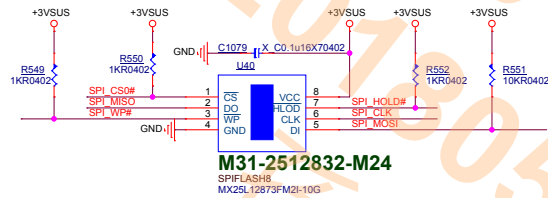
DG/ RTC Well Input Strap

RSMRST# & DSW PWROK, PCH PWROK : PD
RTCRST#, SRTCRST#, INTRUDER# : PU

HM370 (SPI/GPIO)



SPI FLASH ROM



Supported types of Flash Memory
Command: 0x03 & 0x0B & 0xBB

SPIO_I02

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPIO_I03

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPIO_MOSI

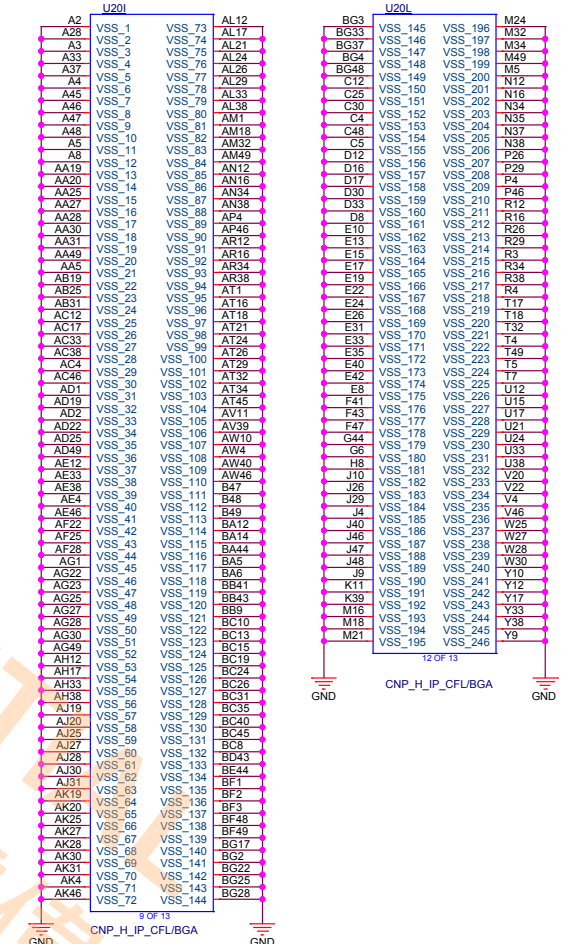
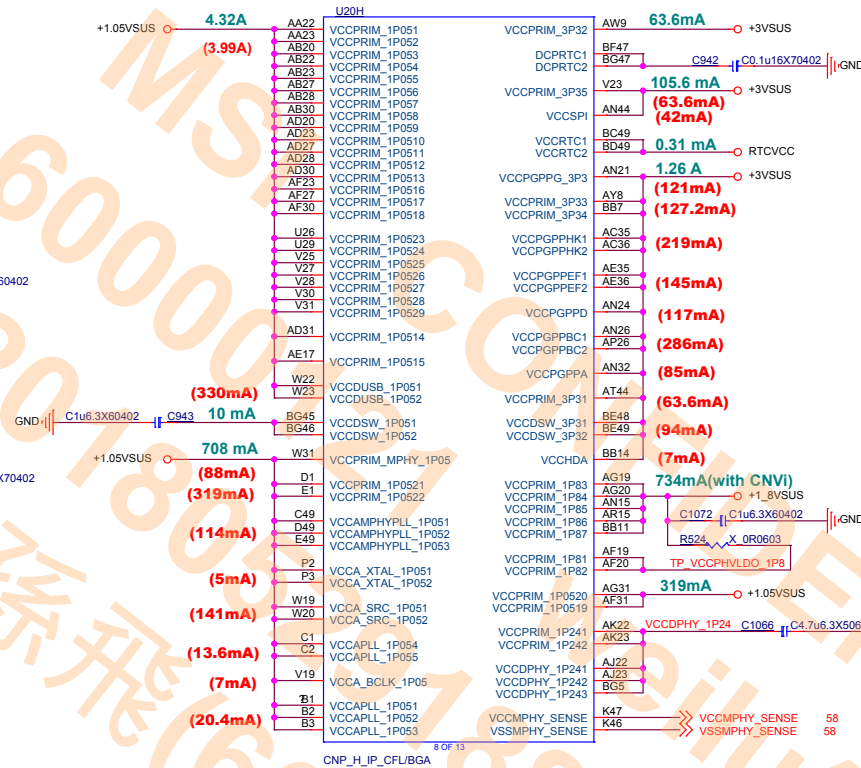
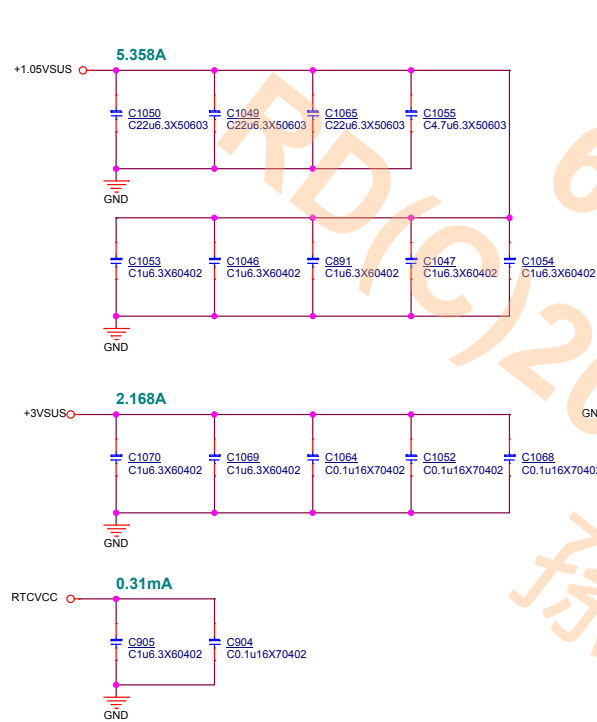
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

DG / Single Flash Topology Table 29-3
(1) R use 50 Ohm for 3.3V
(2) SPIO_I02/I03 PU 1KR when using quad mode

Functional Strap Definitions

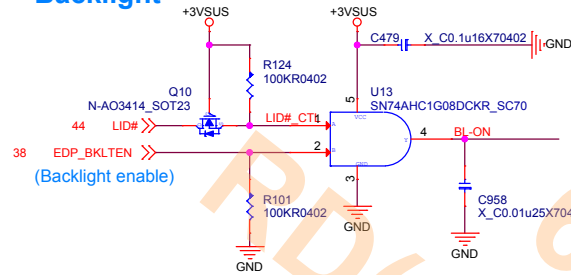
SML3ALERT# / GPP_H15
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
GSPH_MOSI / GPP_B22
This Signal has a weak internal pull-down. Bit 6 Boot BIOS Destination 0 SPI (Default) 1 LPC
GSPH_MOSI / GPP_B18
The signal has a weak internal pull-down. 0 = Disable No Reboot mode. (Default) 1 = Enable No Reboot mode

HM370 (Power & GND)

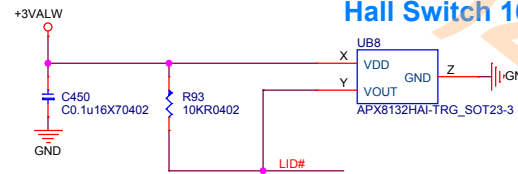


eDP / Camera

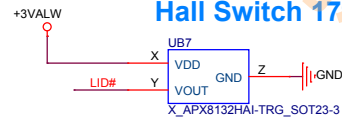
Backlight



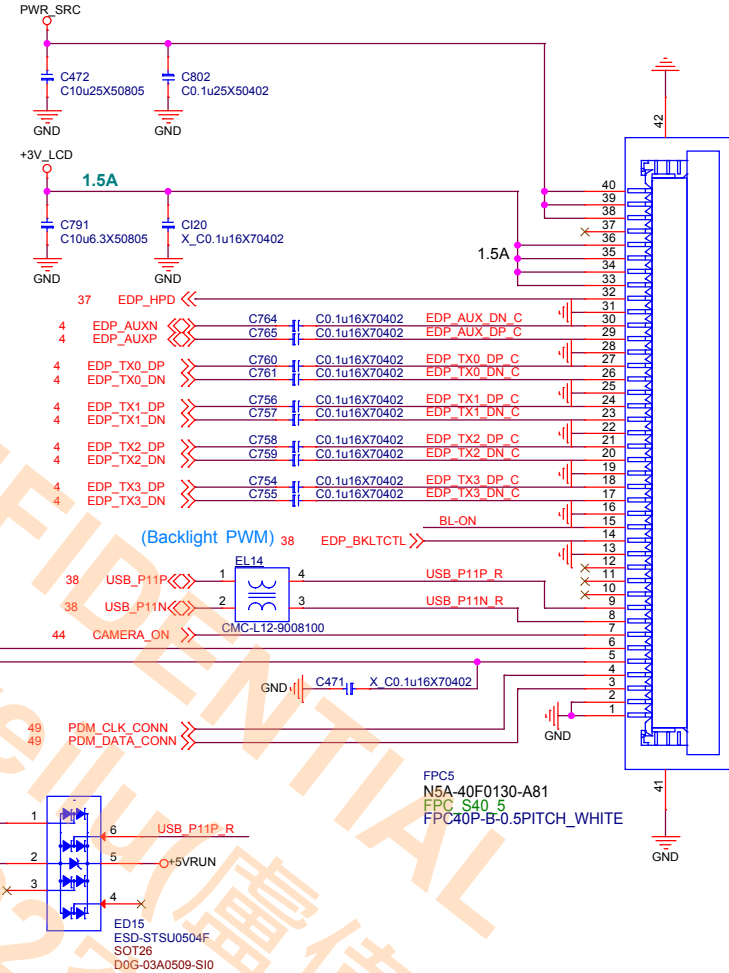
Hall Switch 16JE



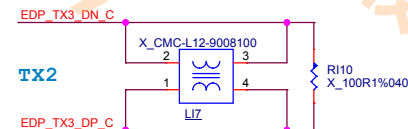
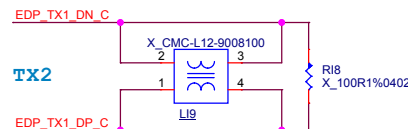
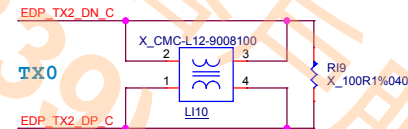
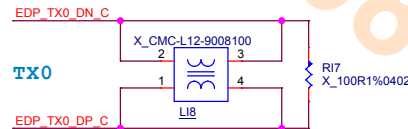
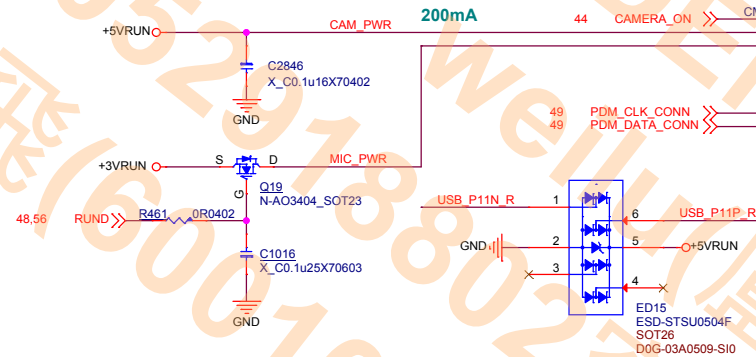
Hall Switch 179E



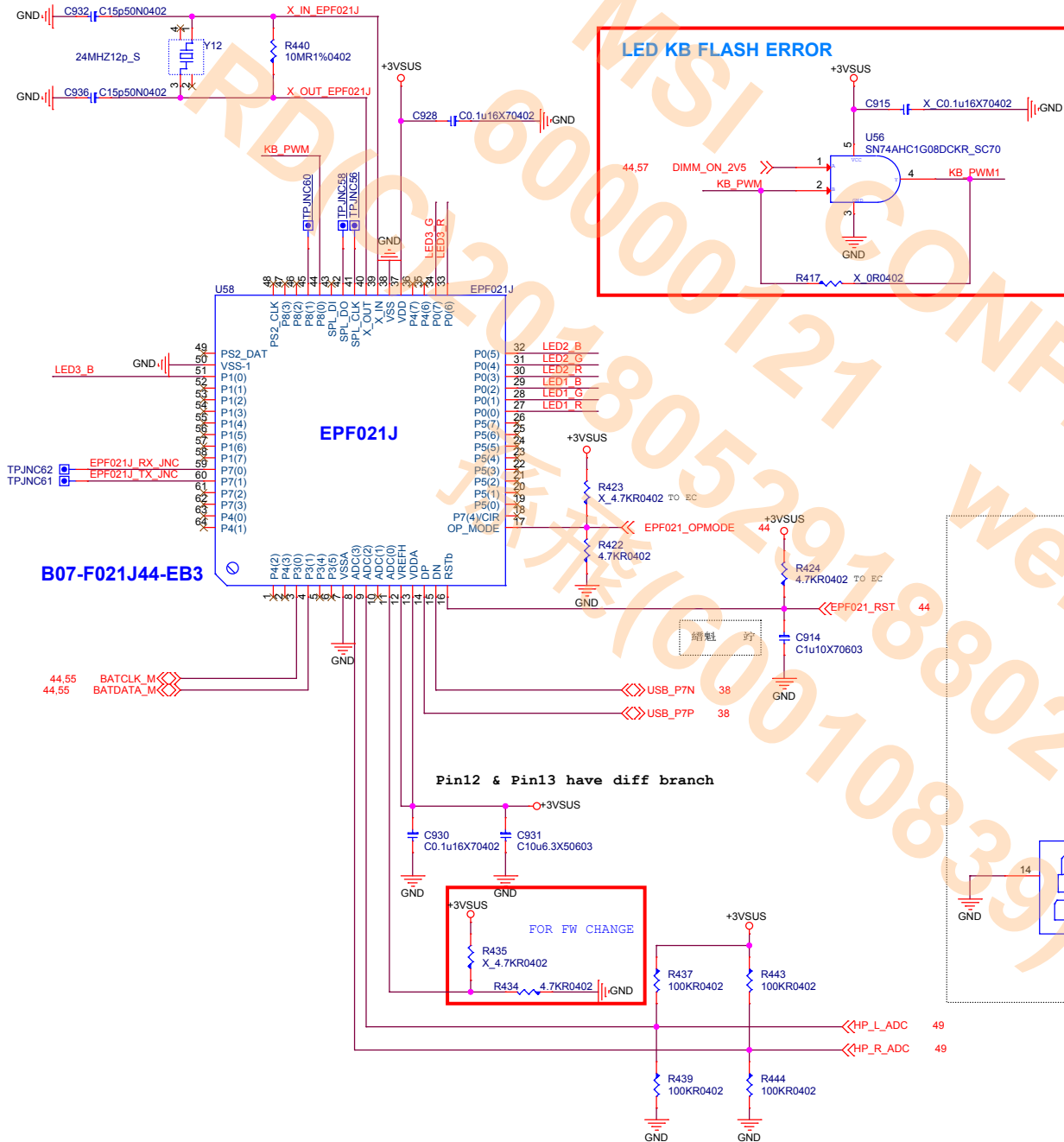
eDP CONN



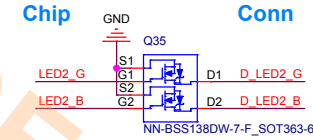
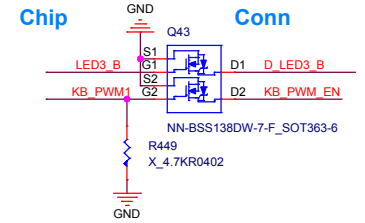
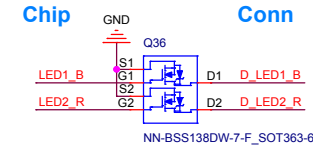
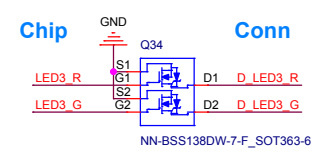
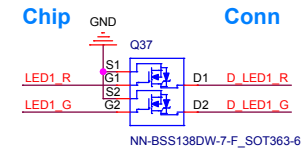
CAMERA



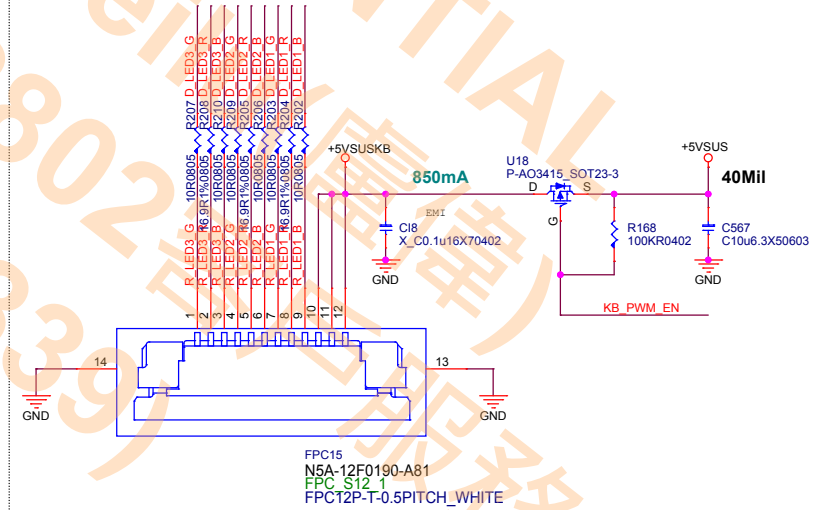
Keyboard LED (EPF021J)



EPF021J Sink current not enough, only using BSS138 (0.22A)



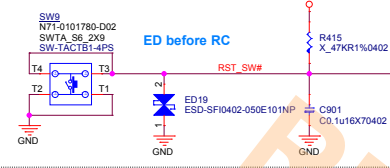
LED Keyboard CONN



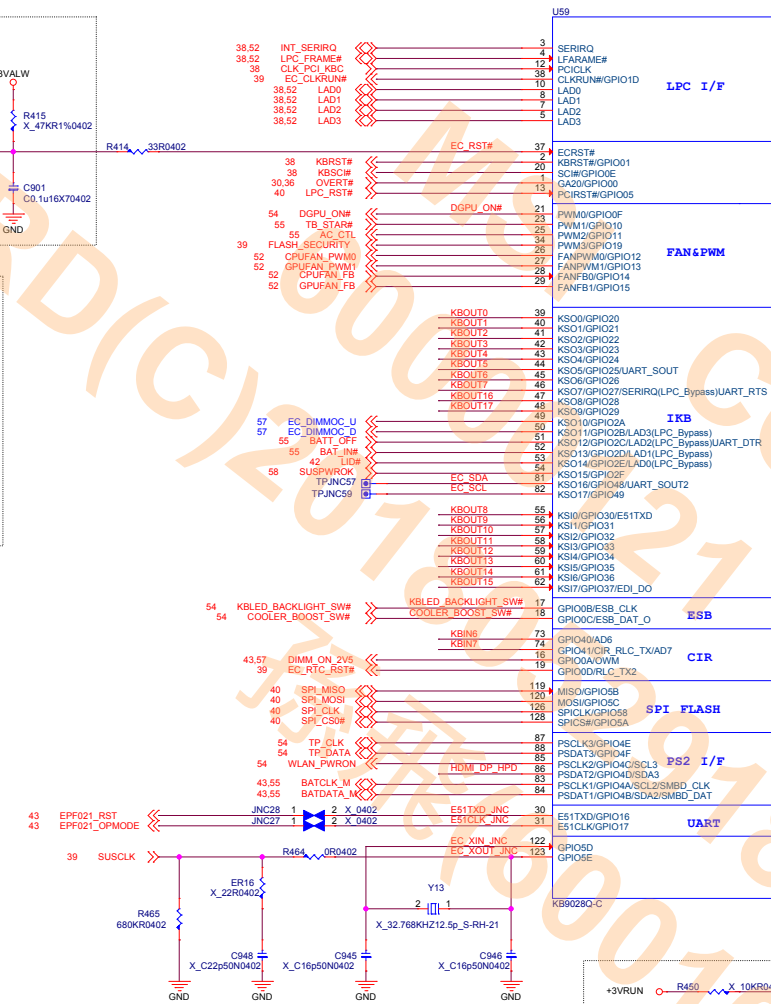
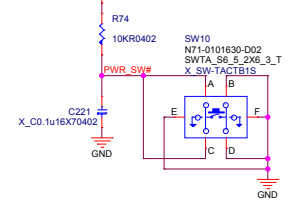
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

KBC/EC/uP (ENE9028)

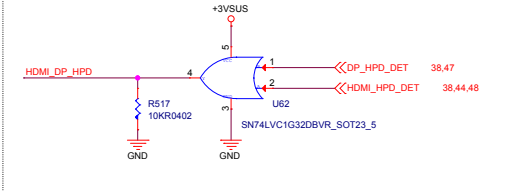
Hardware Reset



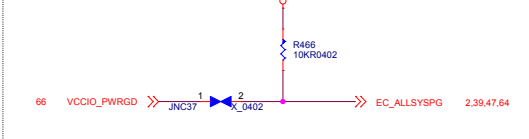
HW Debug



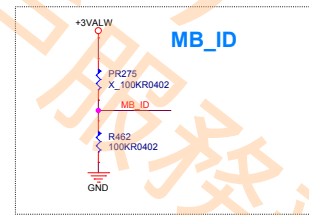
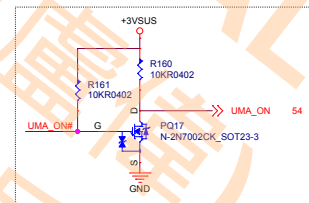
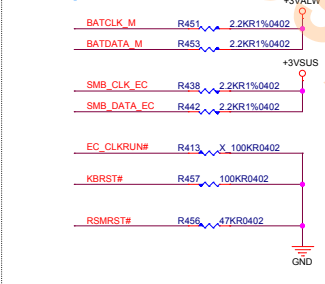
HDMI/DP HPD(Reserved)



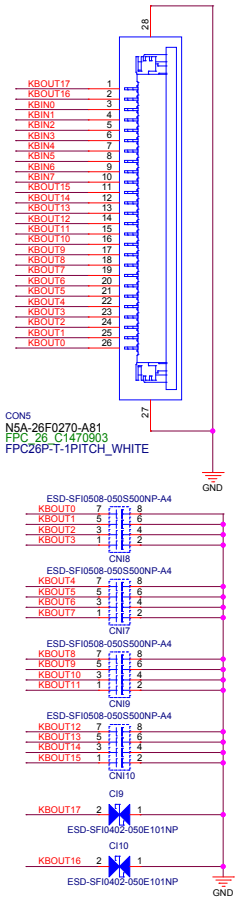
ALLSYSPG



Pull Up/Pull Down



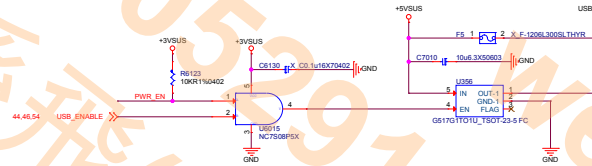
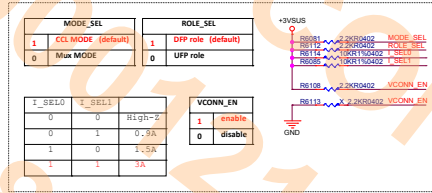
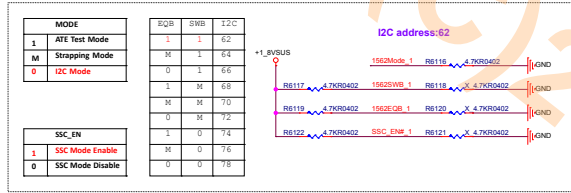
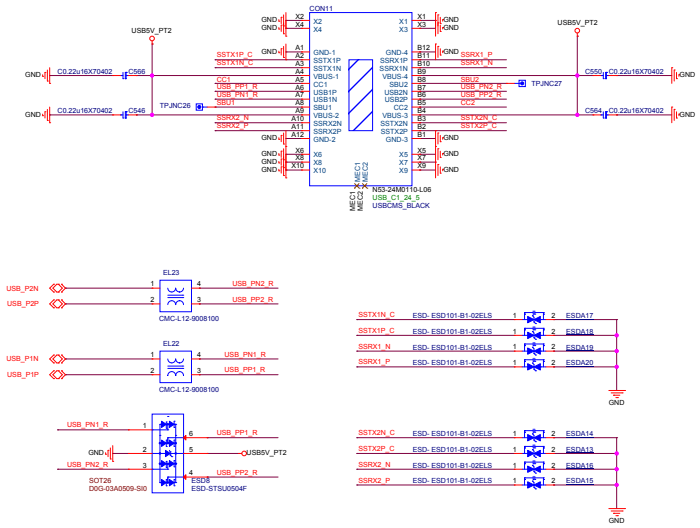
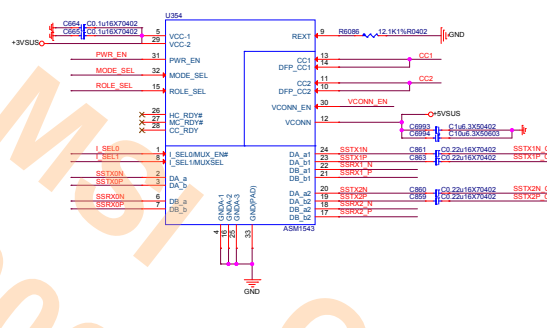
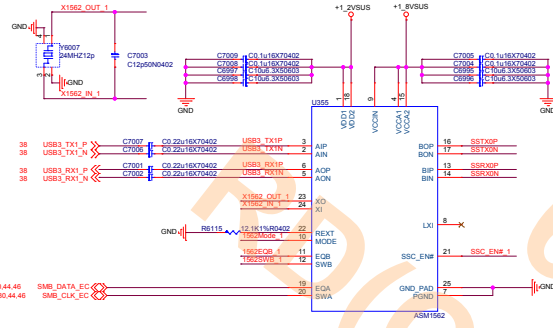
Keyboard conn



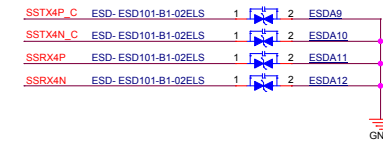
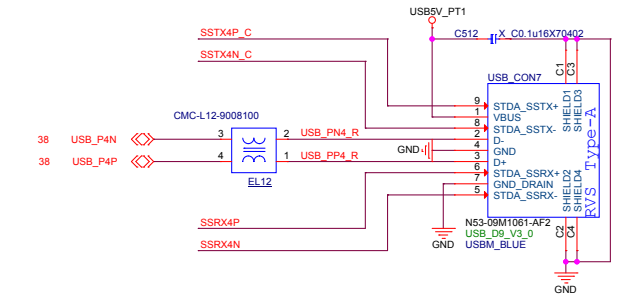
USB3.1 Gne2 Redriver

USB3.1 Gne2 Switch

USB3.1 TYPE C



USB3.1 CNT-1



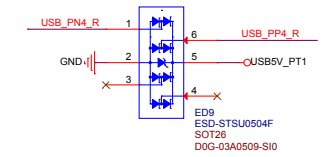
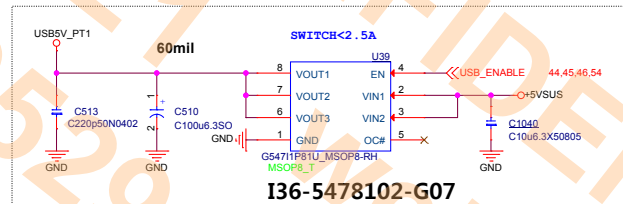
I2C address:78

+1.8V_{SUS}

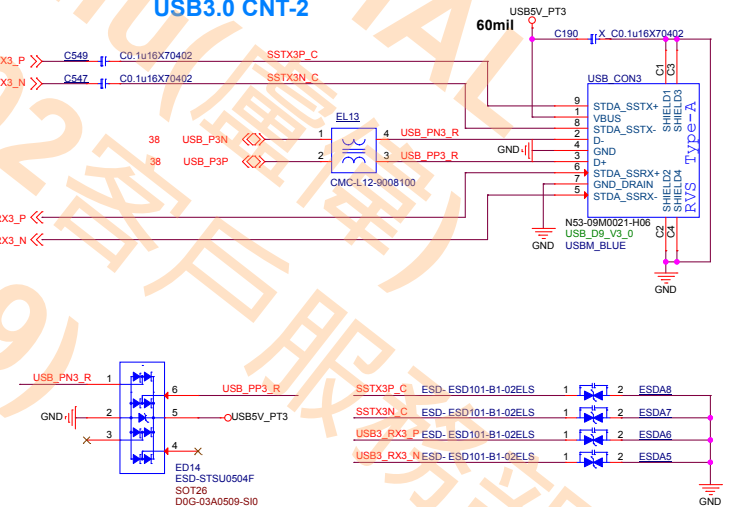
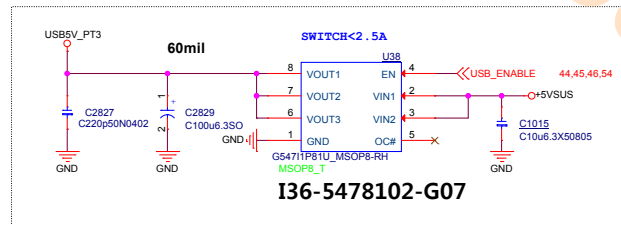
R1300 X 4.7K0402 1562SWB 4 R1301 4.7K0402 | |GND

R1302 X 4.7K0402 1562EOB 4 R1303 4.7K0402 | |GND

R1305 4.7K0402 SSC_EN# 4 R1304 X 4.7K0402 | |GND



I36-5478102-G07

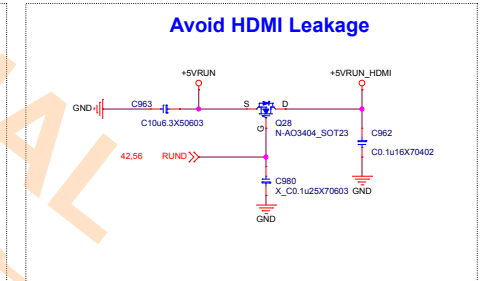
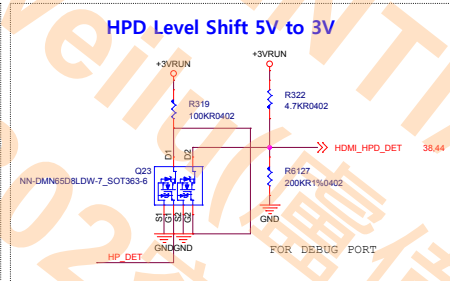
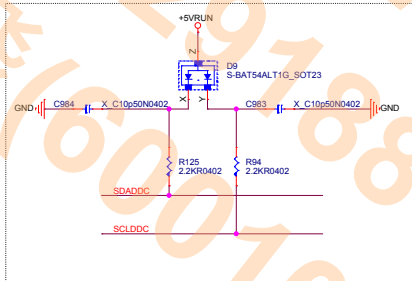
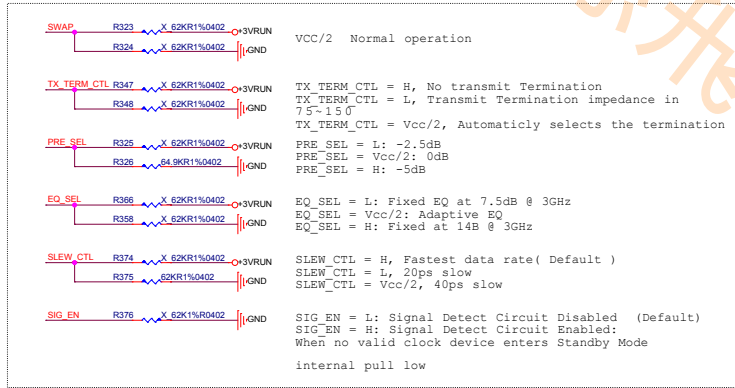
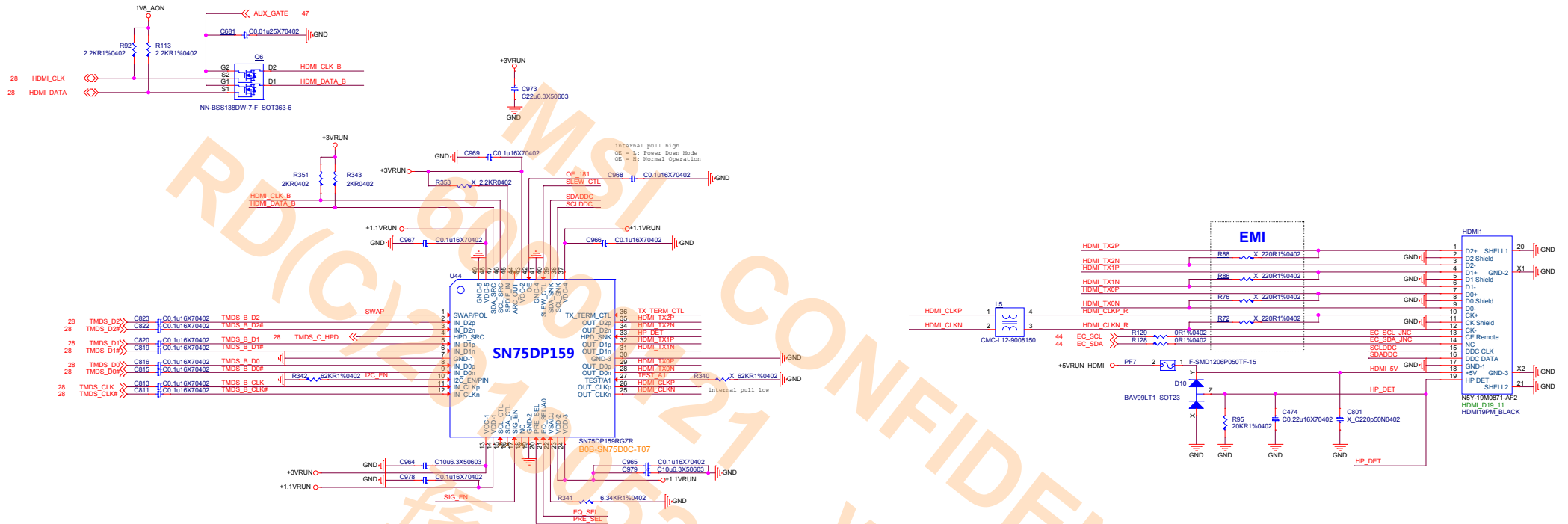


[illegible]

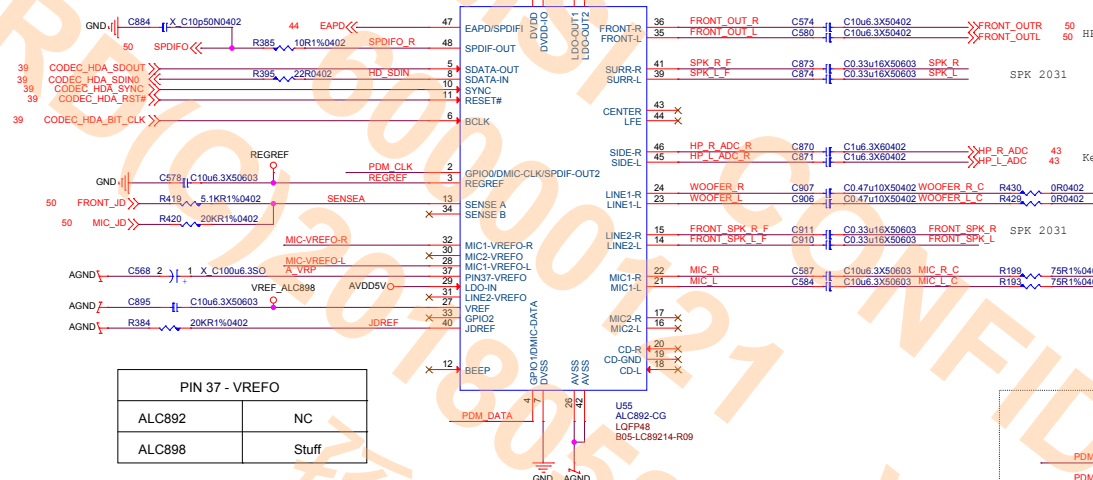
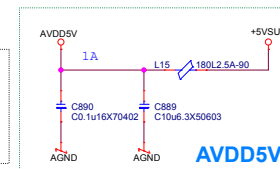
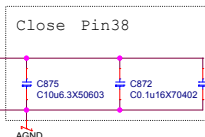
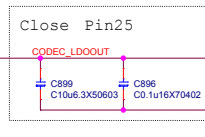
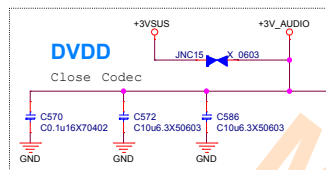
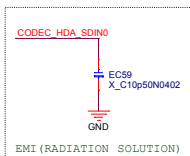
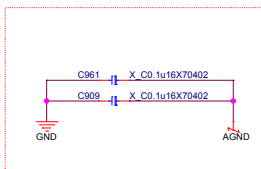
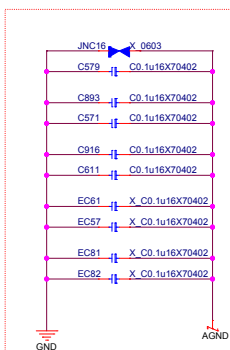
Figure 10 illustrates the connection of the X_CMCMC-L12-9008100 component to the DP and TX pins of four different LAN chips: LANE0, LANE1, LANE2, and LANE3. Each diagram shows a transformer-like component with four pins (1, 2, 3, 4) and a center tap (5). The component is connected to the DP pin via a resistor (ER9, ER8, ER7, ER14) and to the TX pin via a resistor (X_180R1%0402).

- LANE0:** The component is connected to DP_TXP0_C and DP_TXN0_C. The DP pin is connected to pin 2, and the TX pin is connected to pin 4. The center tap (5) is connected to pin 1.
- LANE1:** The component is connected to DP_TXP1_C and DP_TXN1_C. The DP pin is connected to pin 2, and the TX pin is connected to pin 4. The center tap (5) is connected to pin 1.
- LANE2:** The component is connected to DP_TXP2_C and DP_TXN2_C. The DP pin is connected to pin 2, and the TX pin is connected to pin 4. The center tap (5) is connected to pin 1.
- LANE3:** The component is connected to DP_TXP3_C and DP_TXN3_C. The DP pin is connected to pin 2, and the TX pin is connected to pin 4. The center tap (5) is connected to pin 1.

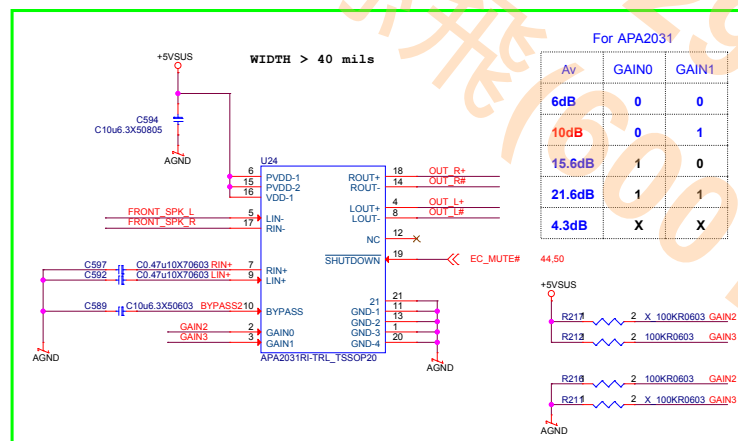
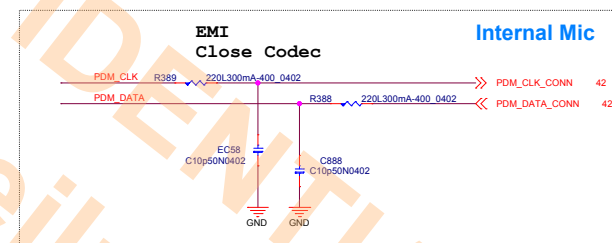
HDMI Level Shifter



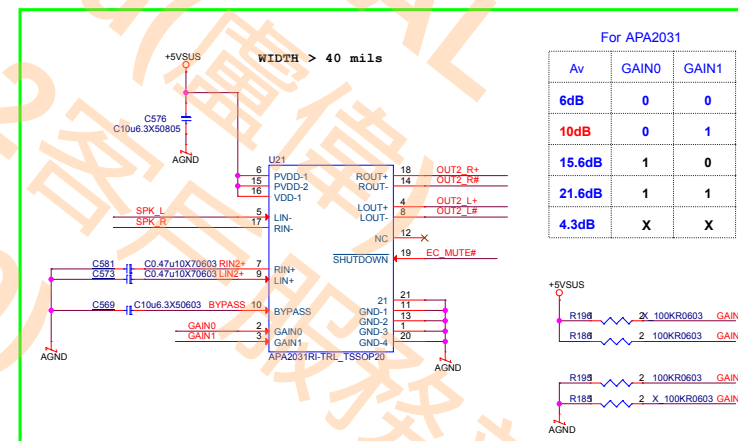
Audio CODEC/Audio AMP



PIN 37 - VREFO	
ALC892	NC
ALC898	Stuff

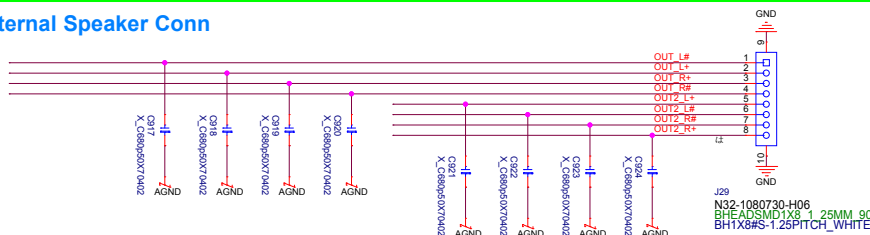


Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X



Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

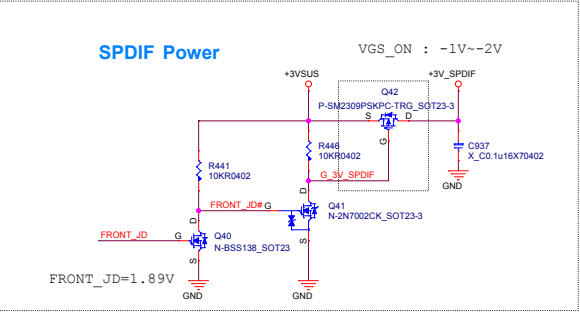
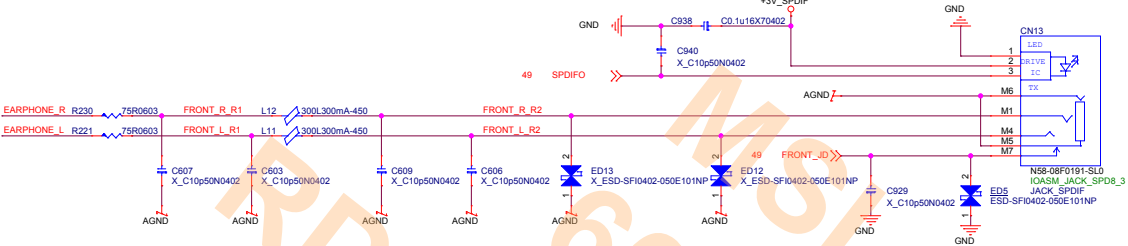
Internal Speaker Conn



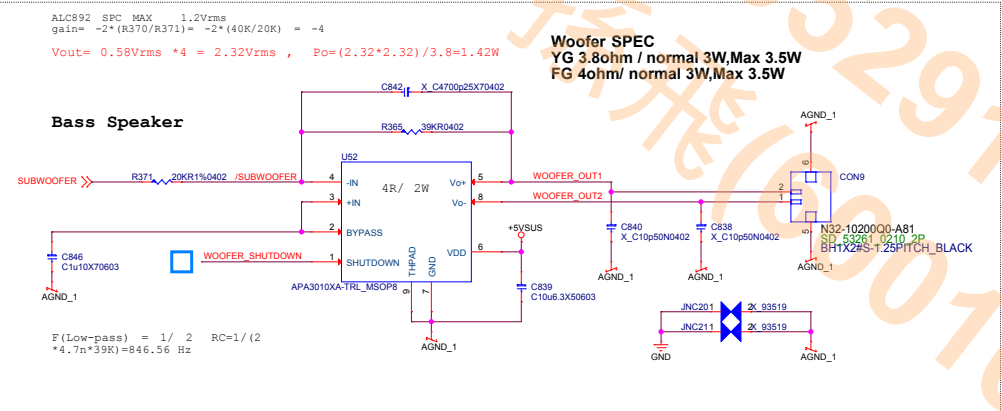
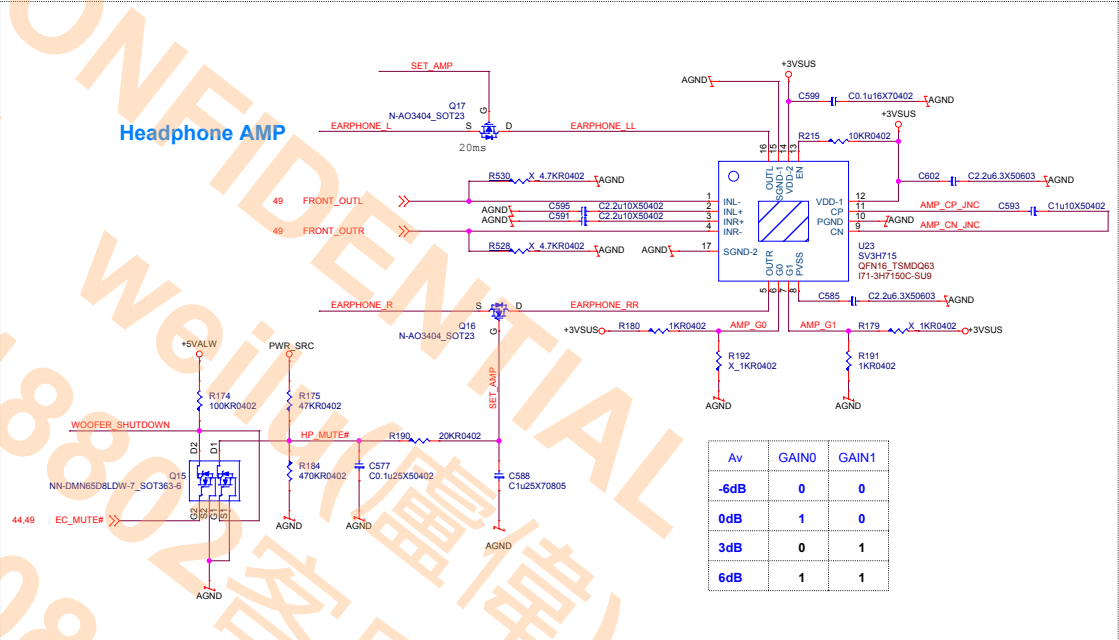
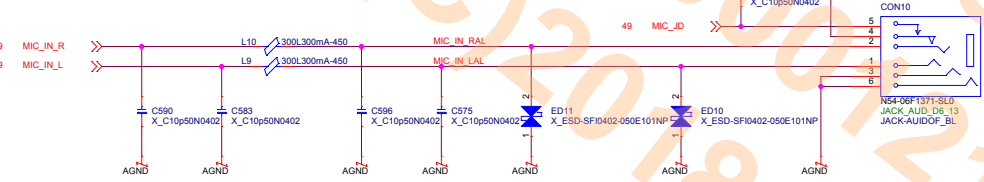
	CODEC	斥
L	-	-
L	+	+
R	+	+
R	-	-
L2	+	+
L2	-	-
R2	-	-
R2	+	+

Audio CONN / Woffler

FRONT OUT

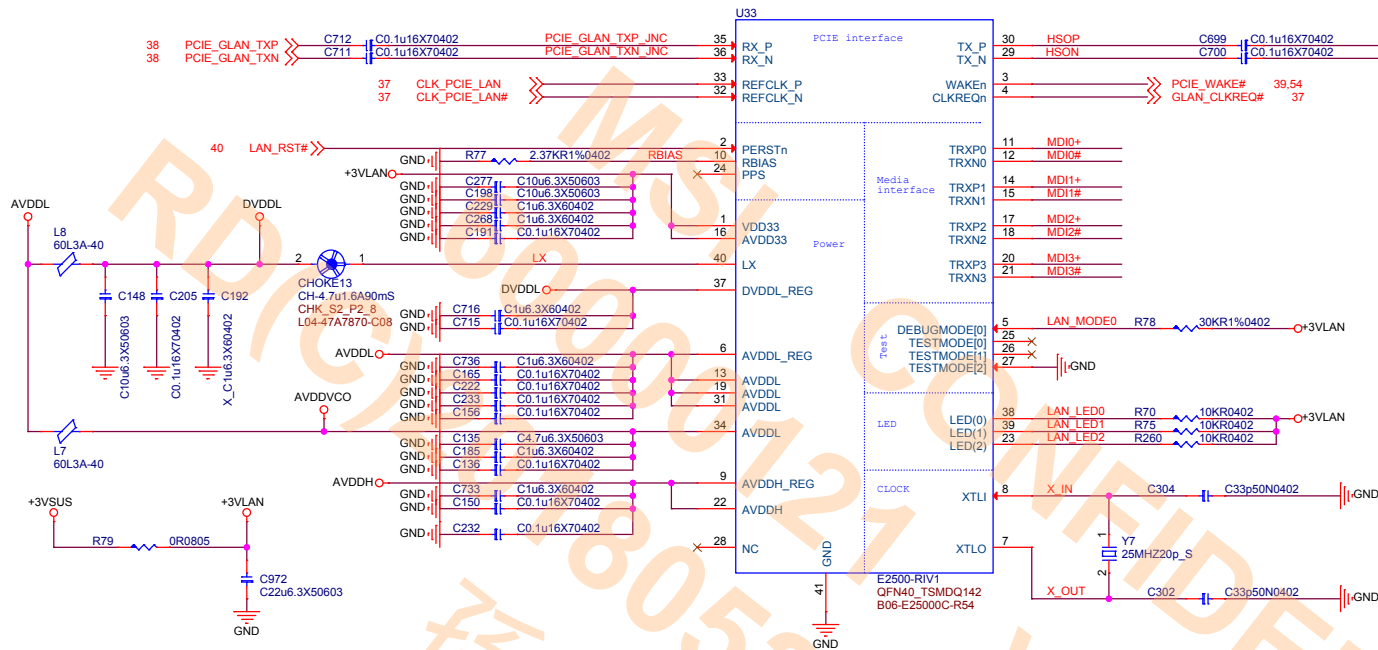


MIC IN

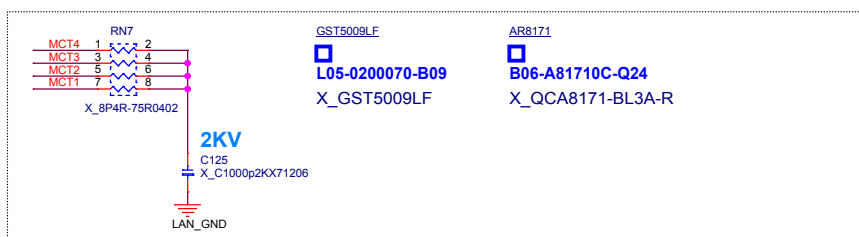
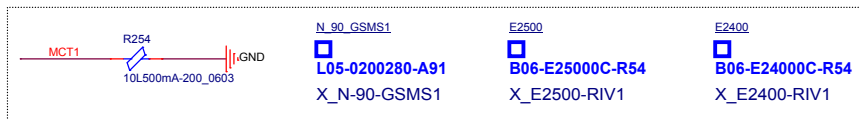
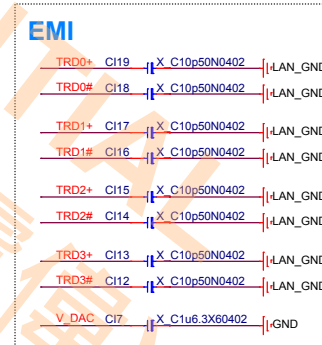
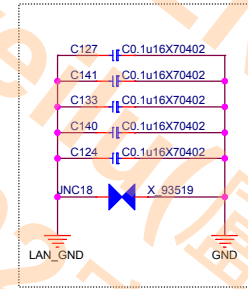
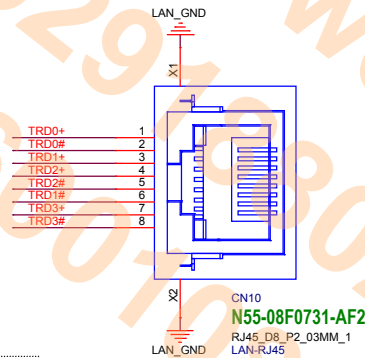
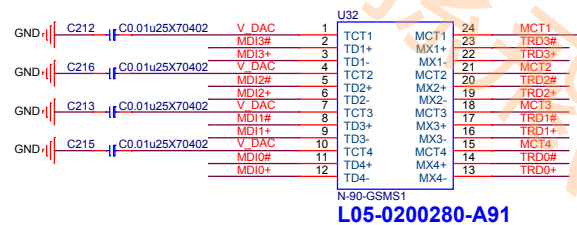


Av	GAIN0	GAIN1
-6dB	0	0
0dB	1	0
3dB	0	1
6dB	1	1

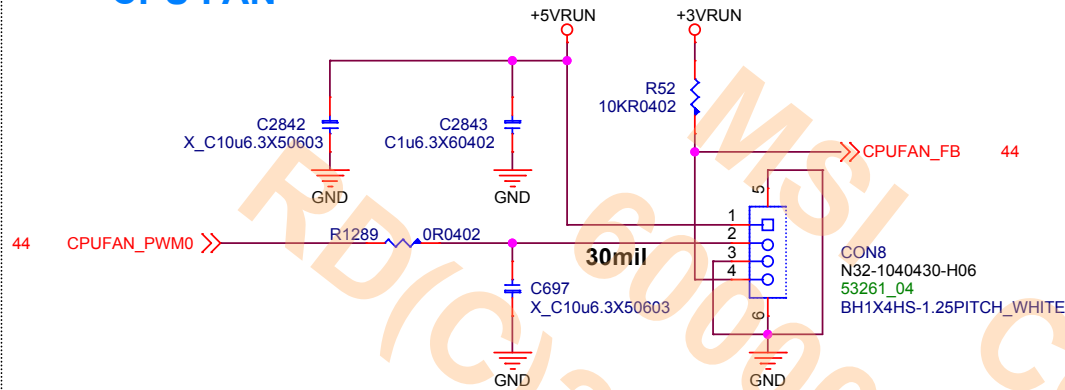
GIGA LAN(BigFoot BFN2500)



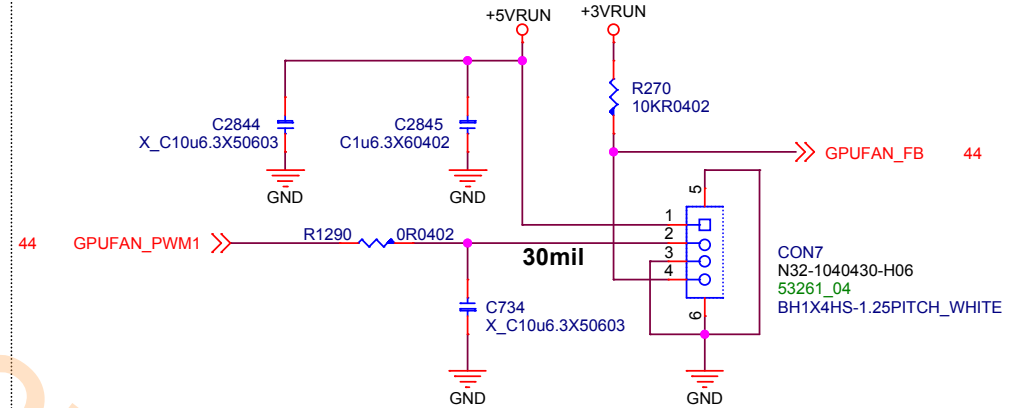
PIN 38 (LAN_LED0)	
AR8171	NC
E2500	Stuff
E2400	Stuff



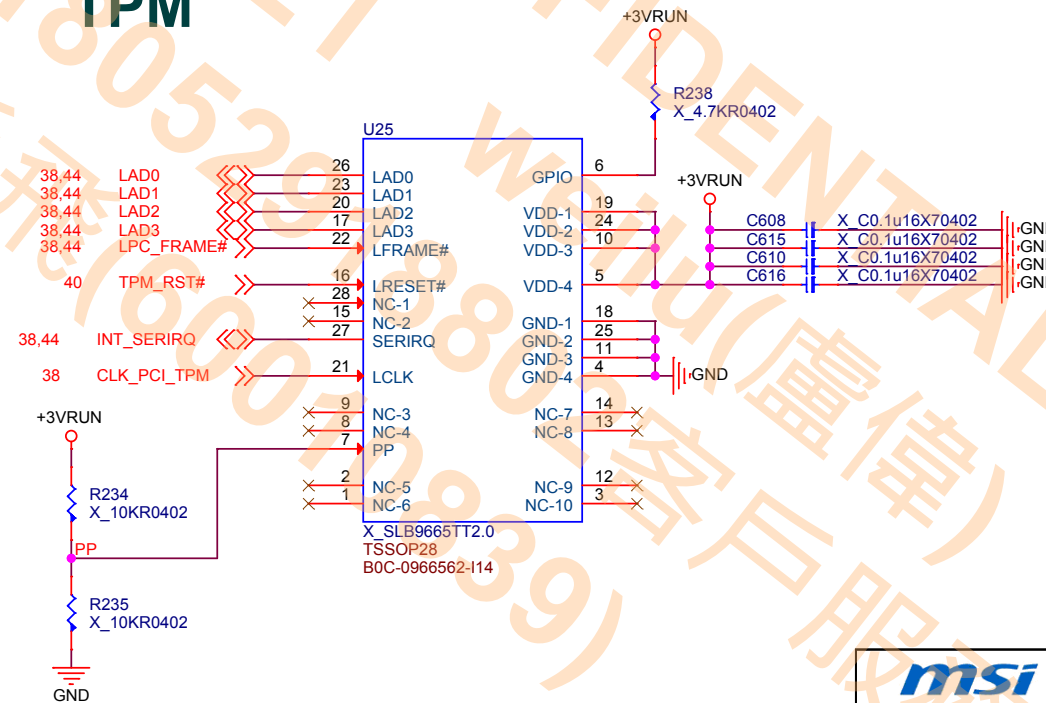
CPU FAN




DGPU FAN

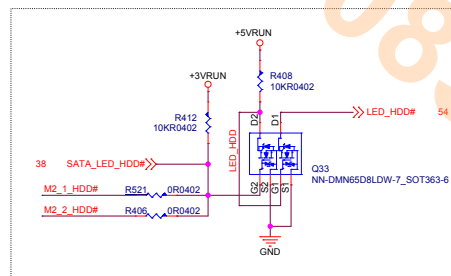
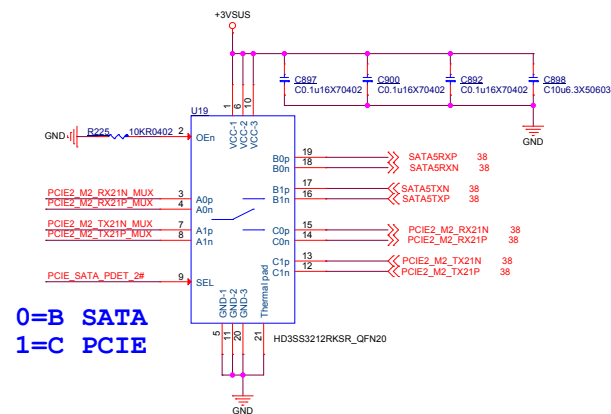
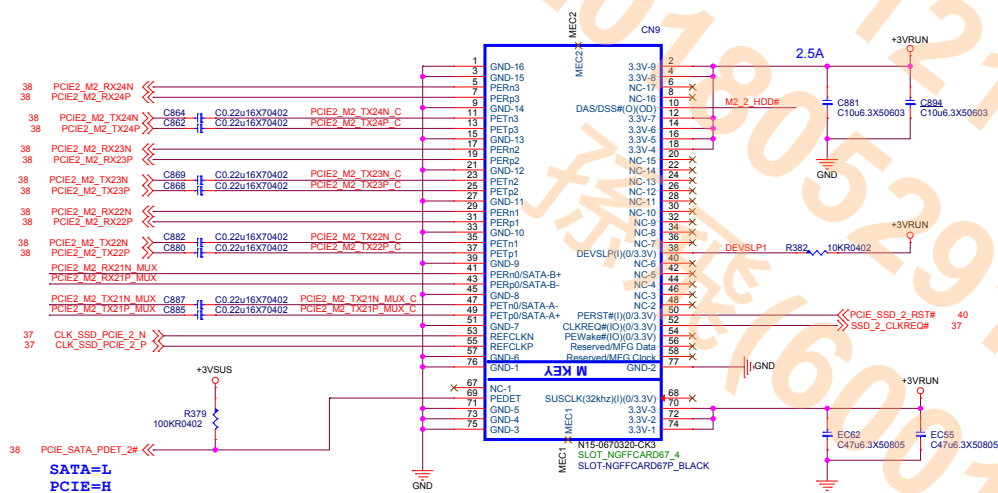
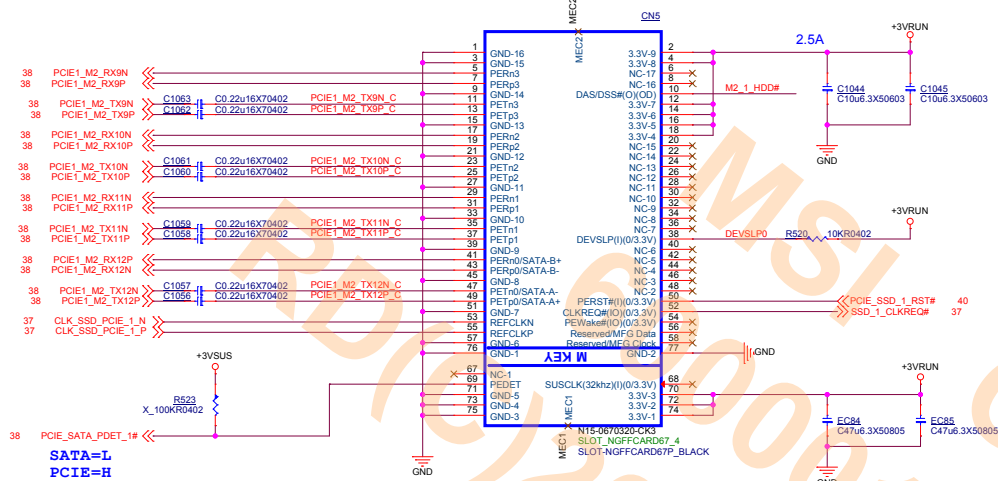


TPM



		MICRO-STAR INT'L CO.,LTD.	
Title			
FAN/TPM			
Size	Document Number		Rev
	MS-16JE		1.0
Date:	Monday, December 25, 2017		Sheet 52 of 75

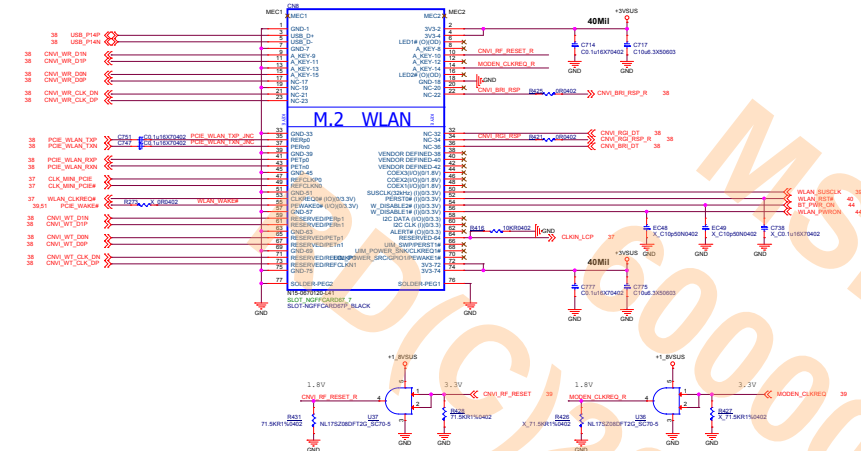
PCIEx4 / SATA M.2 SSD



WLAN / LED / TP / BTB

WLAN

E KEY



Pin #	M.2 WLAN	INTEL CNVI WLAN	Pin #	M.2 WLAN	INTEL CNVI WLAN
Pin 1	GND	GND	Pin 2	3.3V	3.3V
Pin 3	USB_D+	N/C	Pin 4	3.3V	3.3V
Pin 5	USB_D-	N/C	Pin 6	LED1#	LED1#
Pin 7	GND	N/C	Pin 8	Module Key	N/C
Pin 9	Module Key	WGR_D1N	Pin 10	Module Key	RF_RESET_B(1.8V)
Pin 11	Module Key	WGR_D1P	Pin 12	Module Key	N/C
Pin 13	Module Key	GND	Pin 14	Module Key	CLKREQ0(1.8V)
Pin 15	Module Key	WGR_D0N	Pin 16	LED2#	LED2#
Pin 17	N/C	WGR_D0P	Pin 18	GND	GND
Pin 19	N/C	GND	Pin 20	N/C	N/C
Pin 21	N/C	WGR_CLKN	Pin 22	N/C	GRL_RSP1(1.8V)
Pin 23	N/C	WGR_CLKP	Pin 24	Module Key	Module Key
Pin 25	Module Key	Module Key	Pin 26	Module Key	Module Key
Pin 27	Module Key	Module Key	Pin 28	Module Key	Module Key
Pin 29	Module Key	Module Key	Pin 30	Module Key	Module Key
Pin 31	Module Key	Module Key	Pin 32	N/C	RGL_D1T(1.8V)
Pin 33	GND	GND	Pin 34	N/C	RGL_RSP1(1.8V)
Pin 35	PERP0	N/C	Pin 36	N/C	BGL_D1T(1.8V)
Pin 37	PERN0	N/C	Pin 38	N/C	N/C
Pin 39	GND	GND	Pin 40	N/C	N/C
Pin 41	PETP0	N/C	Pin 42	N/C	N/C
Pin 43	PETN0	N/C	Pin 44	N/C	N/C
Pin 45	GND	GND	Pin 46	N/C	N/C
Pin 47	REFCLKP0	N/C	Pin 48	N/C	N/C
Pin 49	REFCLKN0	N/C	Pin 50	SUSCLK (32KHz)	SUSCLK (32KHz)
Pin 51	GND	GND	Pin 52	PERST0#	N/C
Pin 53	CLKREQ0#	N/C	Pin 54	BT_EN (W_DISABLE2#)	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	N/C	Pin 56	WLAN_EN (W_DISABLE2#)	WLAN_EN (W_DISABLE2#)
Pin 57	GND	GND	Pin 58	N/C	N/C
Pin 59	N/C	WT_D1N	Pin 60	N/C	N/C
Pin 61	N/C	WT_D1P	Pin 62	N/C	N/C
Pin 63	GND	GND	Pin 64	Resever	REFCLK0(38.4MHz)
Pin 65	N/C	WT_D0N	Pin 66	N/C	N/C
Pin 67	N/C	WT_D0P	Pin 68	N/C	N/C
Pin 69	GND	GND	Pin 70	N/C	N/C
Pin 71	N/C	WT_CLKN	Pin 72	3.3V	3.3V
Pin 73	N/C	WT_CLKP	Pin 74	3.3V	3.3V
Pin 75	GND	GND			

16JE LED

FRONT

BLUE (HDD)

BLUE (WLAN)

ORANGE (BATLOW)

BLUE (CHARGE)

BLUE (CAP)

16JE LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

DOC-04018F0-L05

179E LED

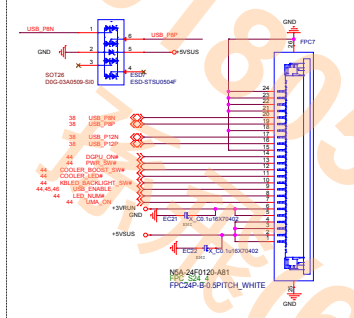
DOC-04018F0-L05

179E LED

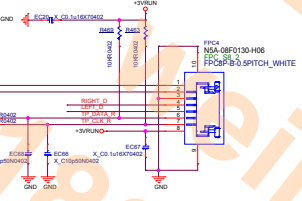
DOC-04018F0-L05

179E LED

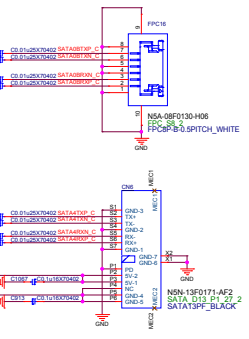
To 16JB2 (Power Board/USB2.0/Card Reader Board)



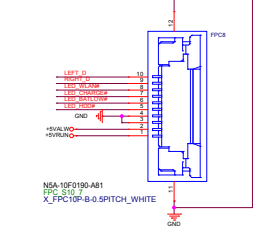
Touch Pad



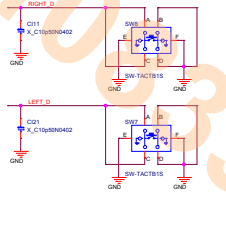
SATA Board To Board



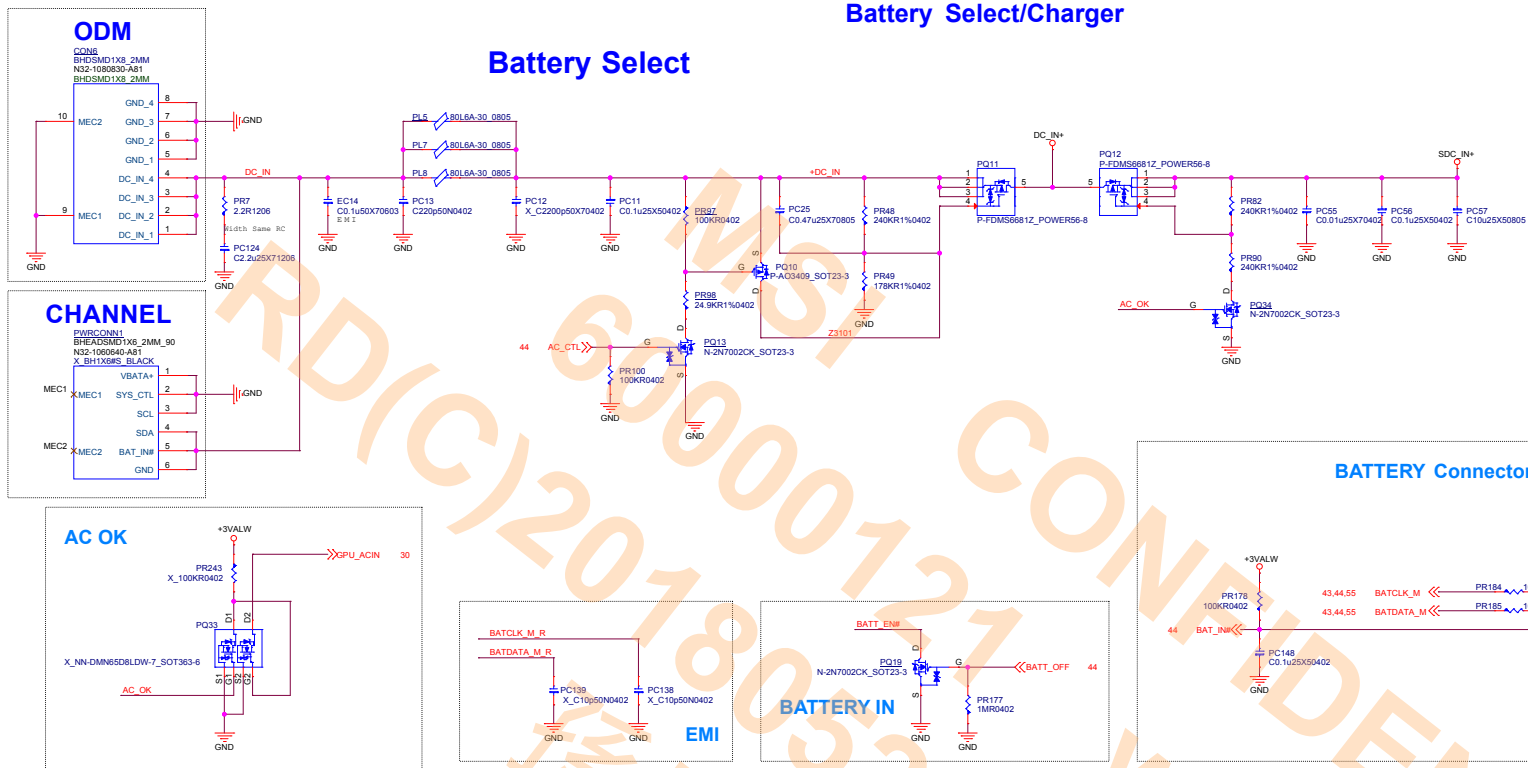
To 179EB (LED / TP Switch Board)



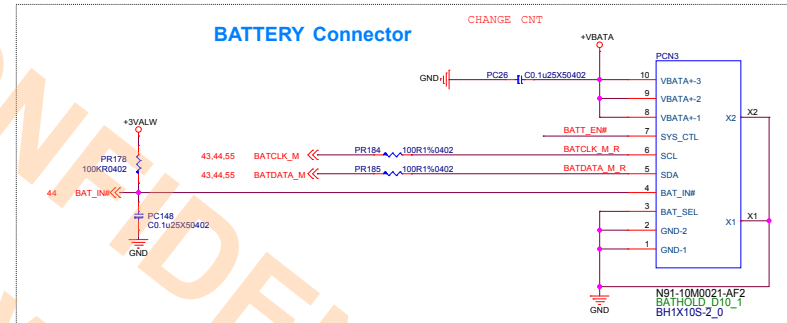
16JE Touch Pad Switch



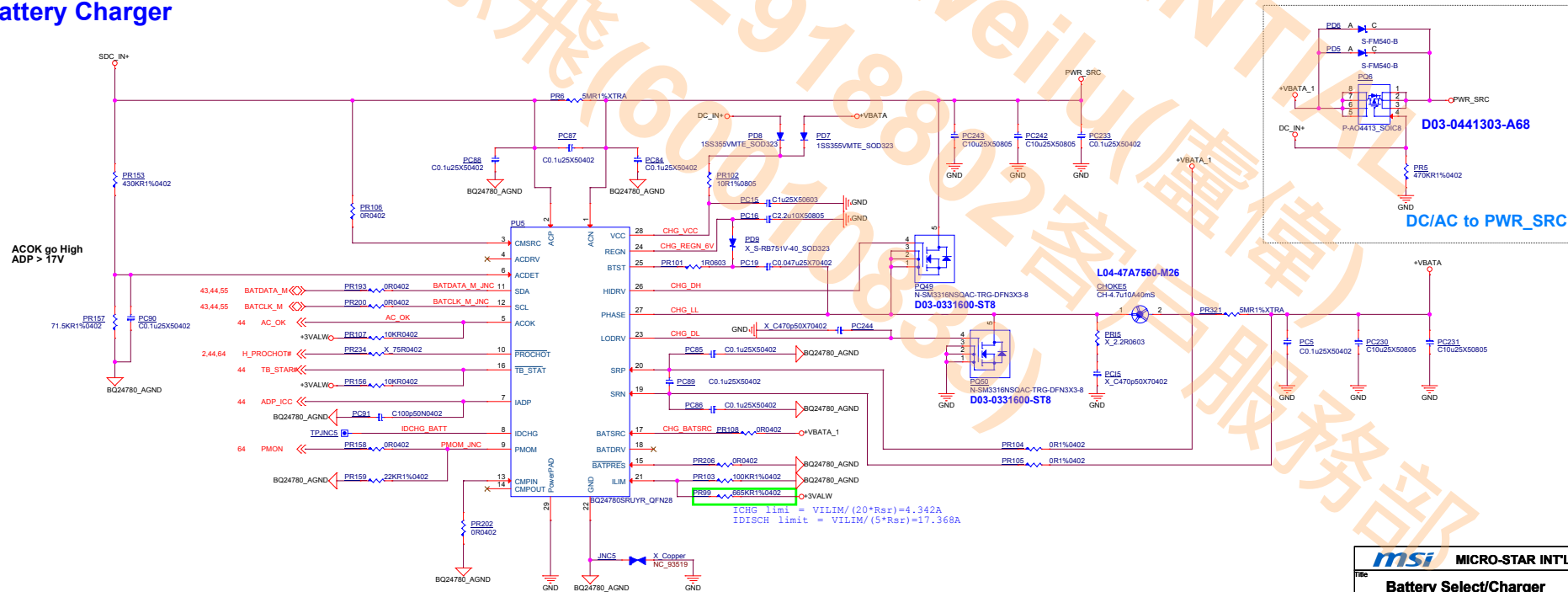
Battery Select



BATTERY Connector



Battery Charger



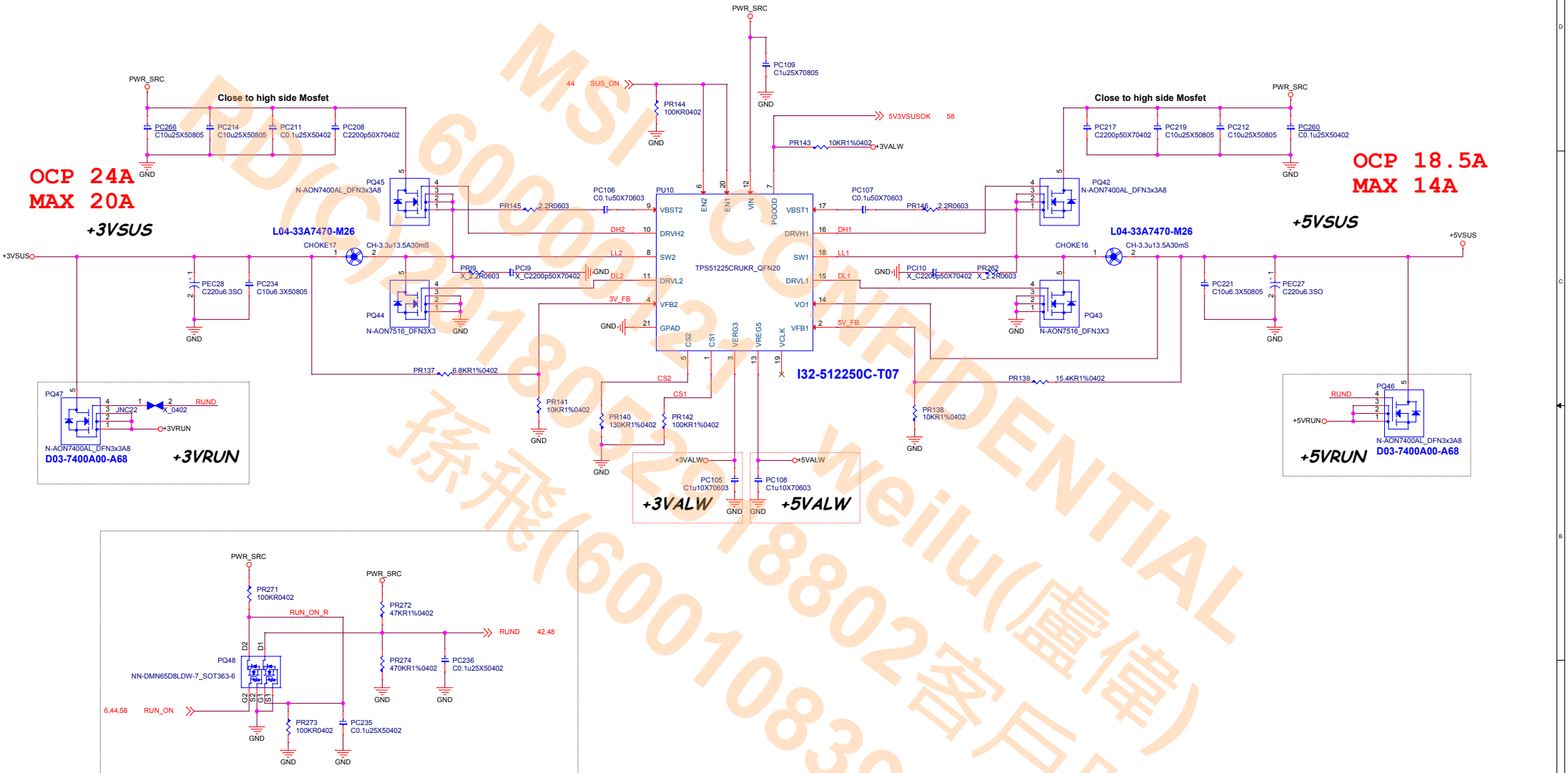
System Power

OCF 24A
MAX 20A

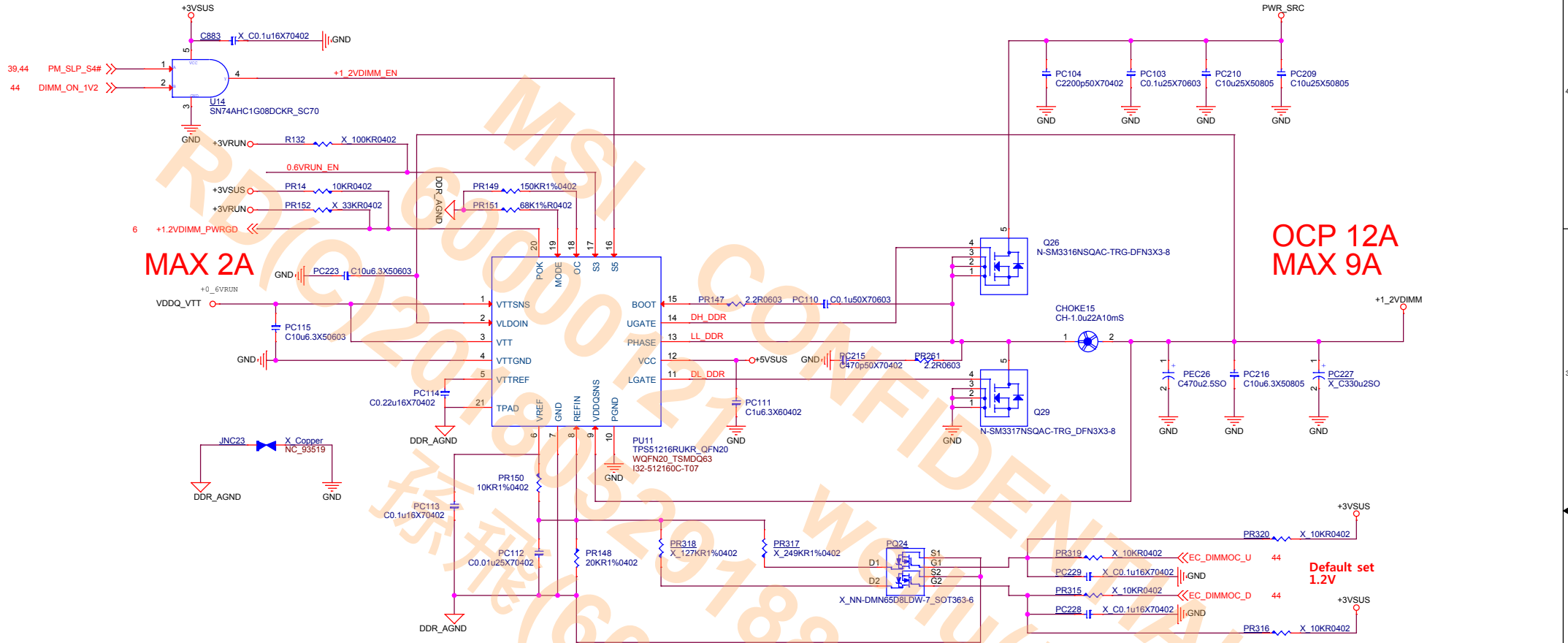
+3VSUS

OCF 18.5A
MAX 14A

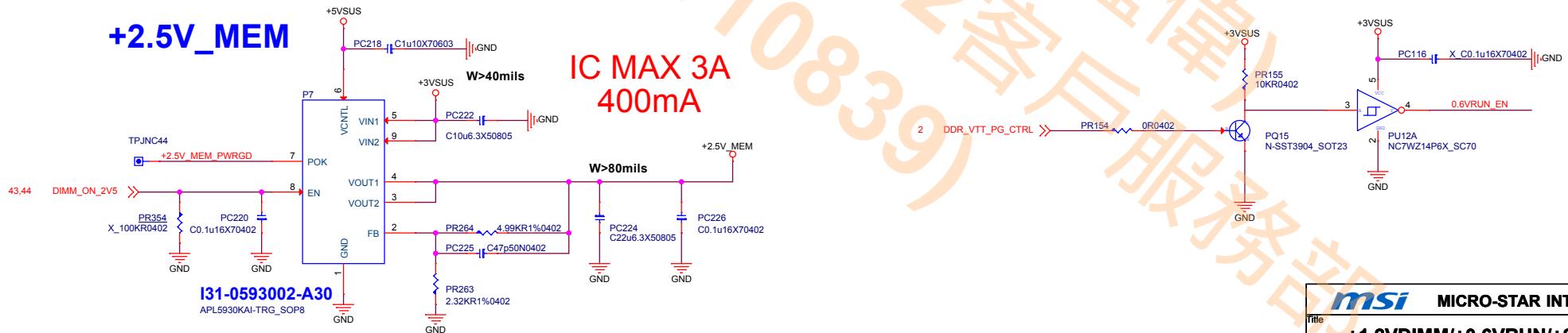
+5VSUS



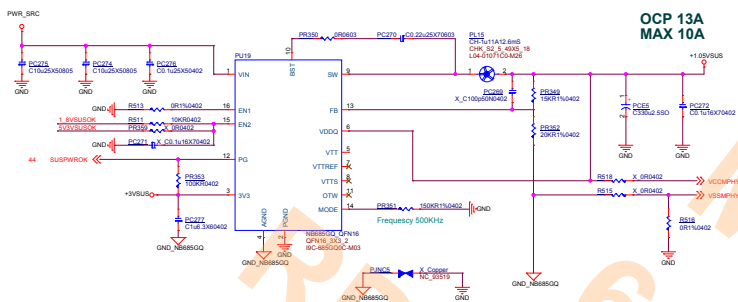
+1_2VDIMM/+0.6VRUN



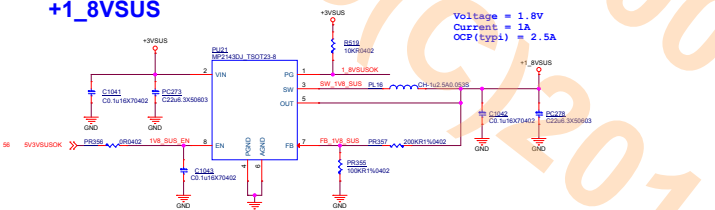
+2.5V_MEM



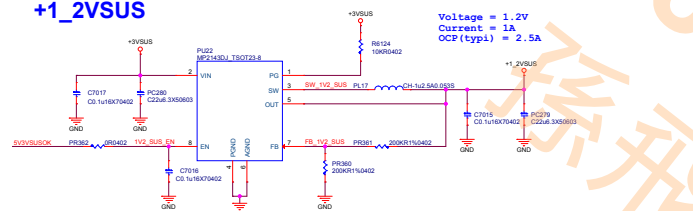
+1.05VSUS



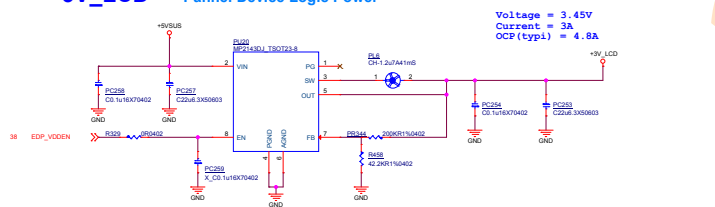
+1_8VSUS



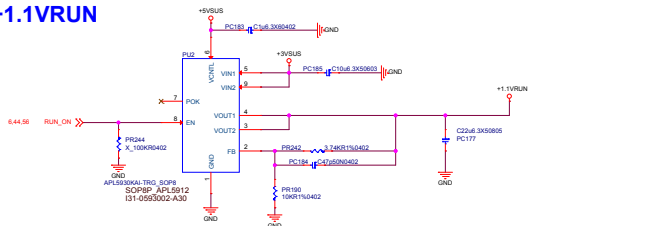
+1_2VSUS



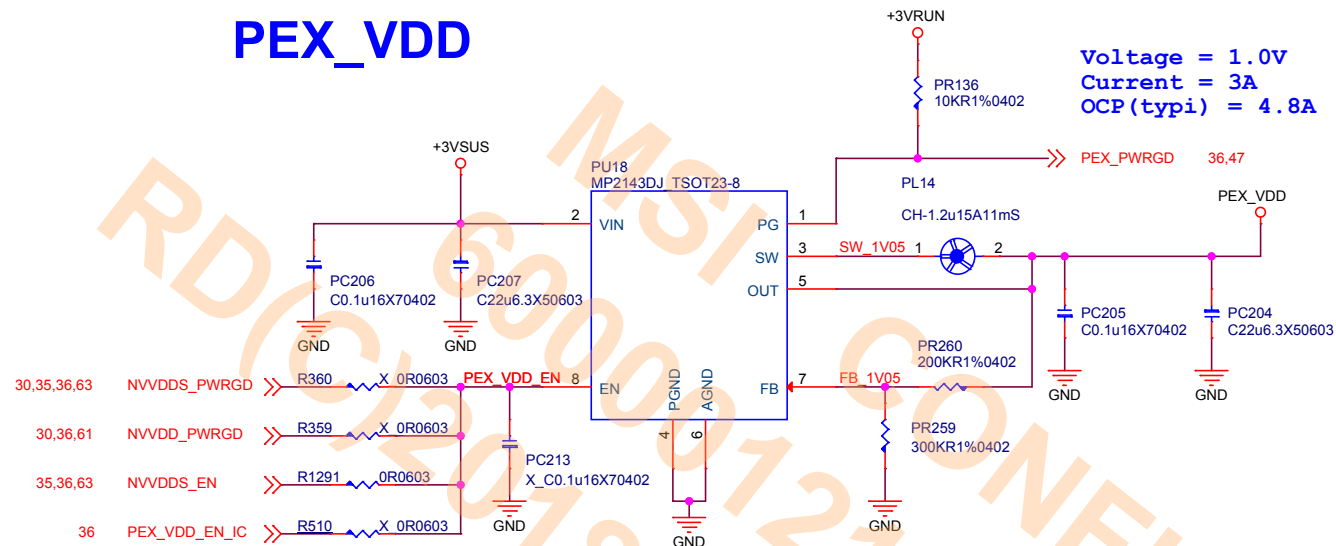
+3V_LCD Pannel Device Logic Power



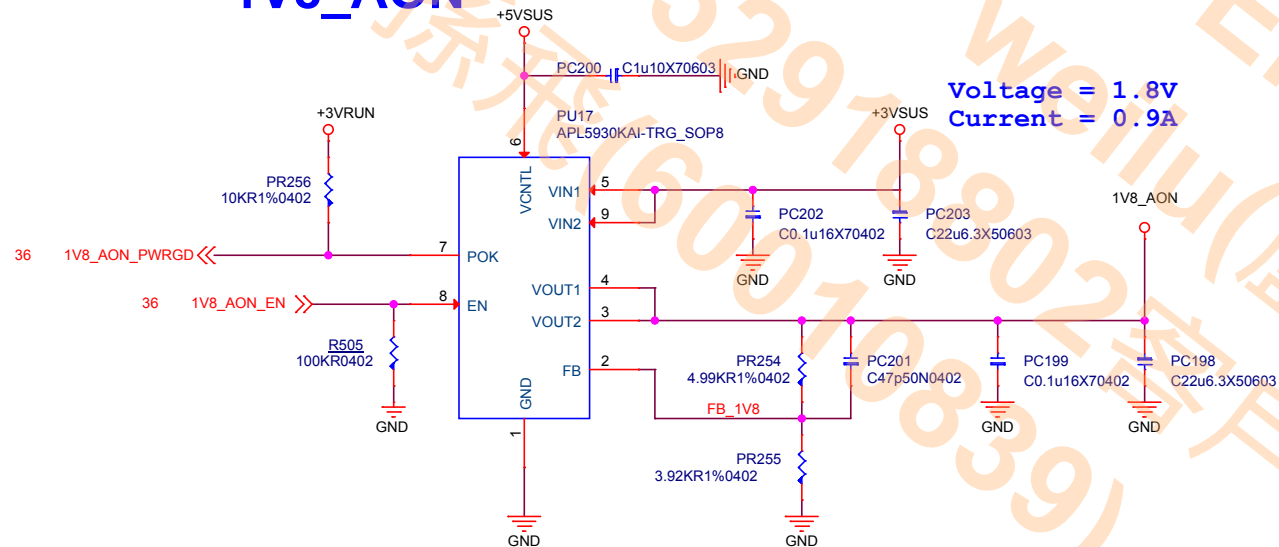
+1.1V RUN



PEX_VDD



1V8_AON



msi

MICRO-STAR INT'L CO.,LTD.

Title **PEX_VDD / 1V8_AON**

Size Document Number

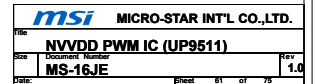
MS-16JE

Rev

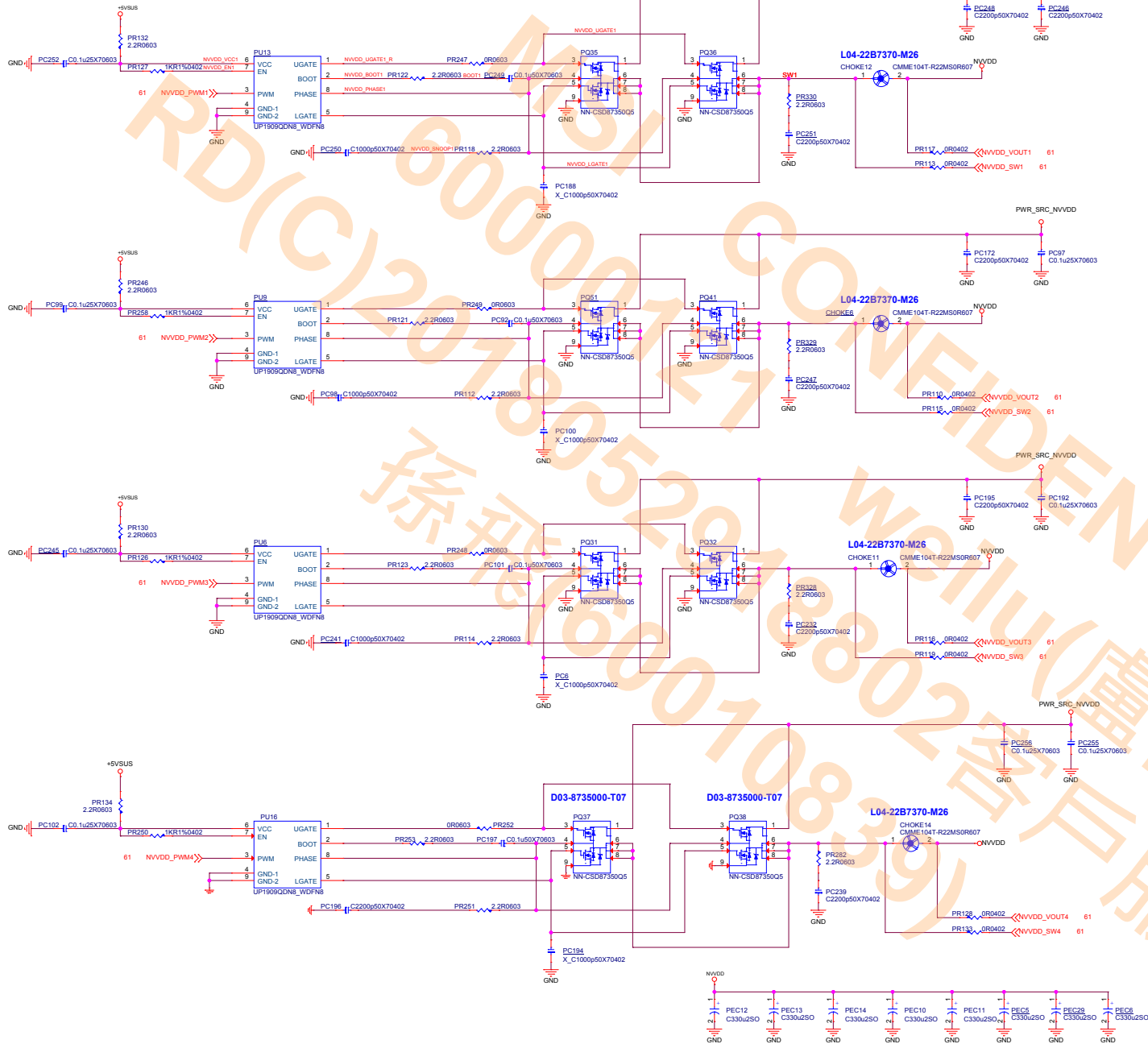
1.0

Date: Monday, December 25, 2017 Sheet 59 of 75

EDP-Peak 300A
EDP-Con 125A



NVDD Phase1~4 (Config A)



msi MICRO-STAR INT'L CO.,LTD.

File NVDD phase1~4

Size Document Number MS-16JE

Rev 1.0

Date Sheet 62 of 75

DGPU POWER / UP1666P

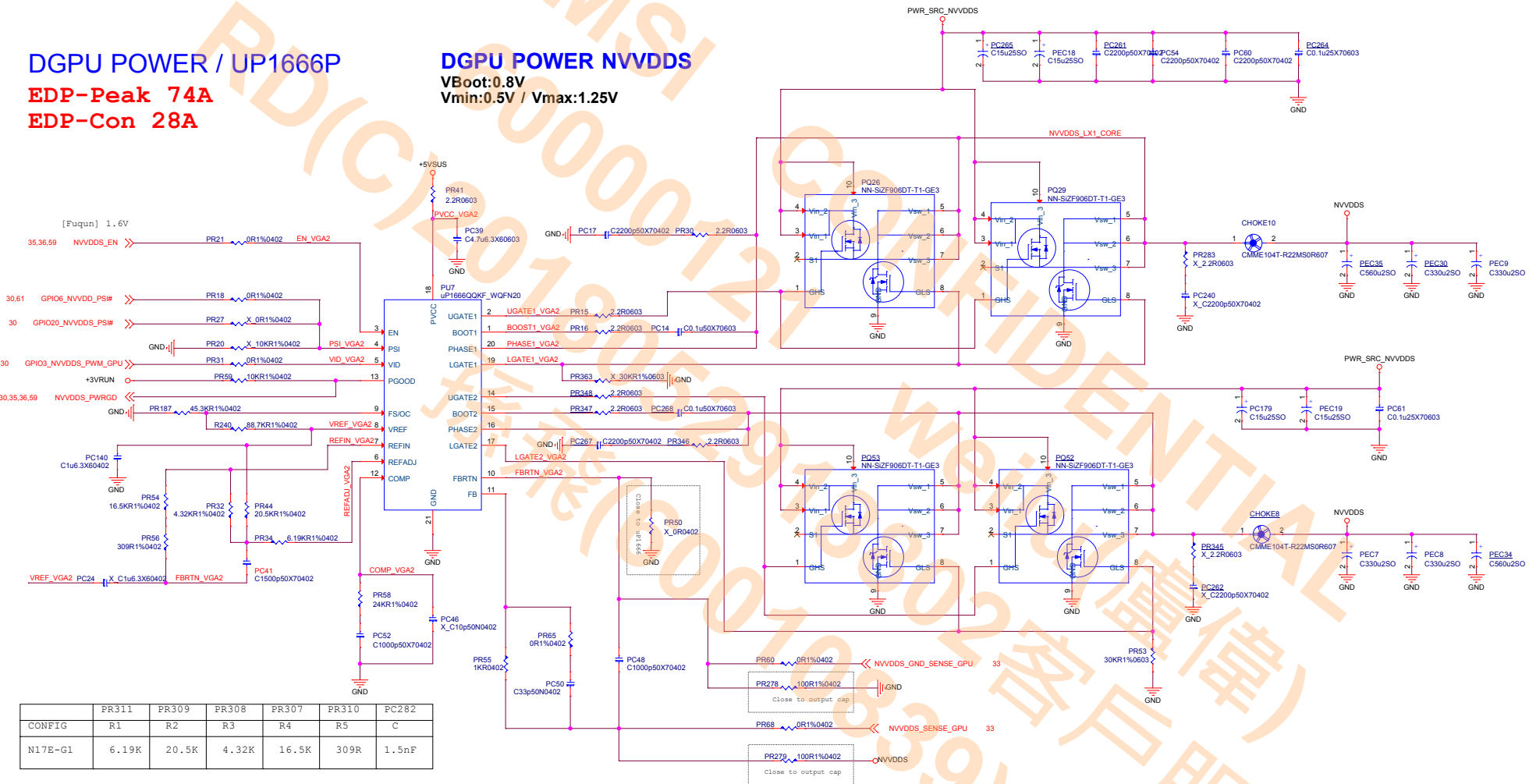
EDP-Peak 74A

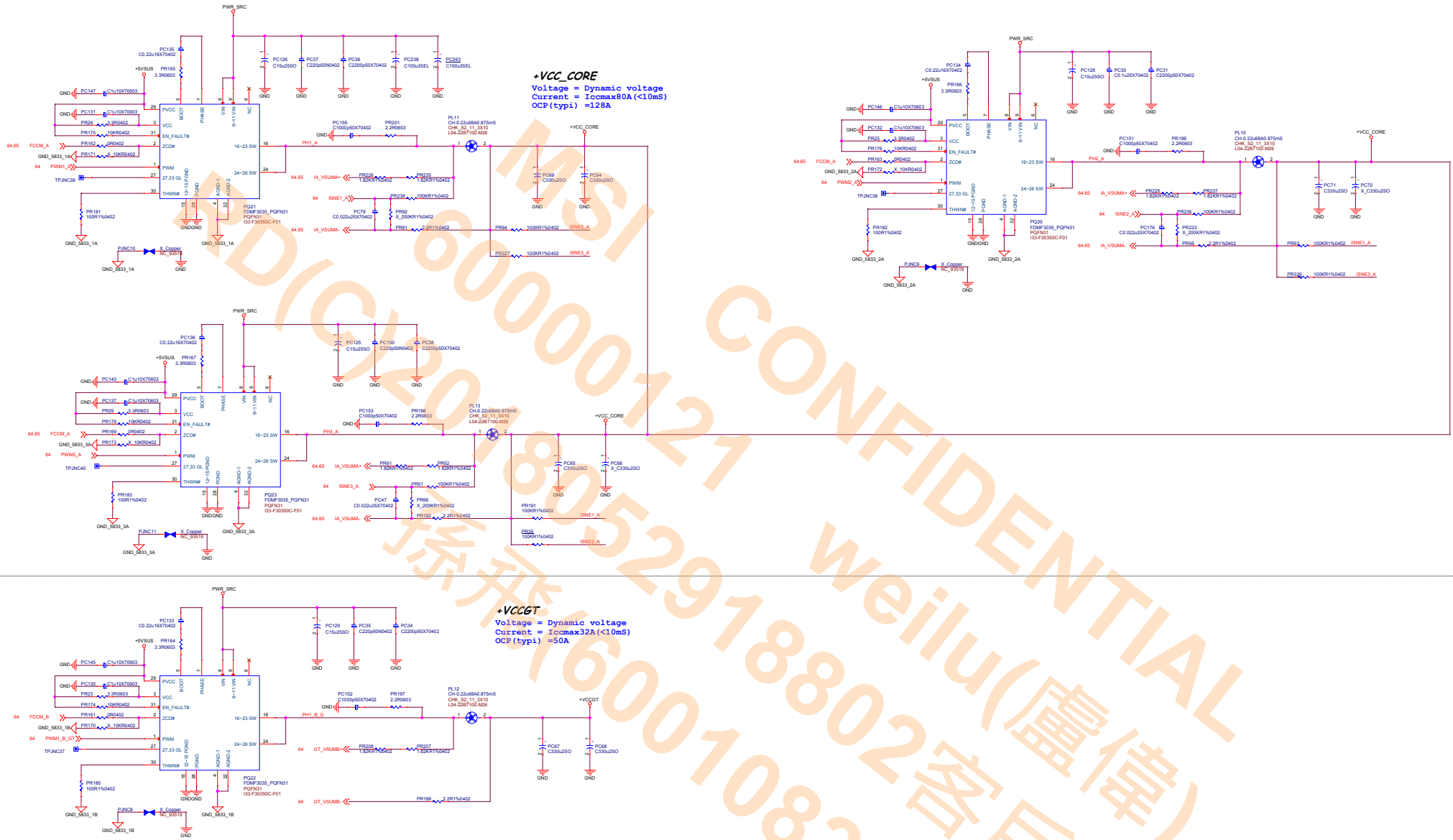
EDP-Con 28A

DGPU POWER NVVDDS

VBoot:0.8V

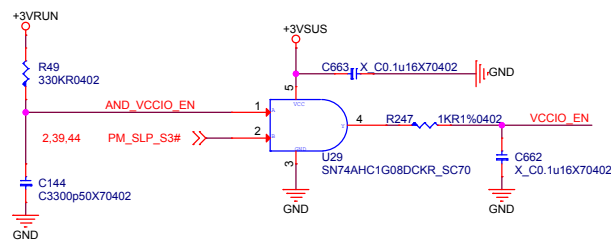
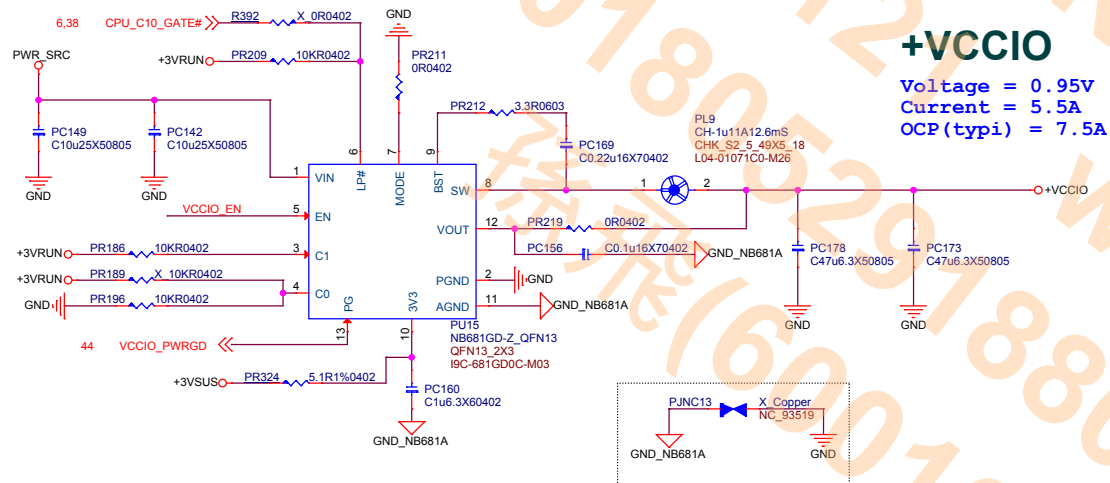
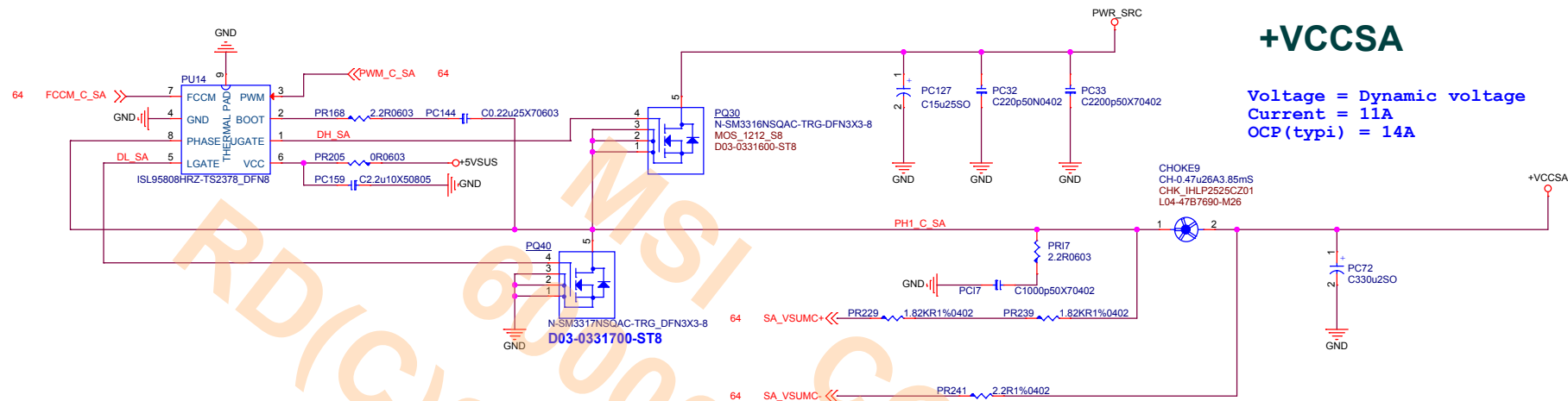
Vmin:0.5V / Vmax:1.25V

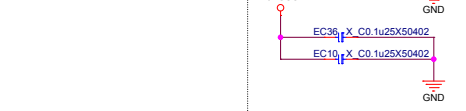
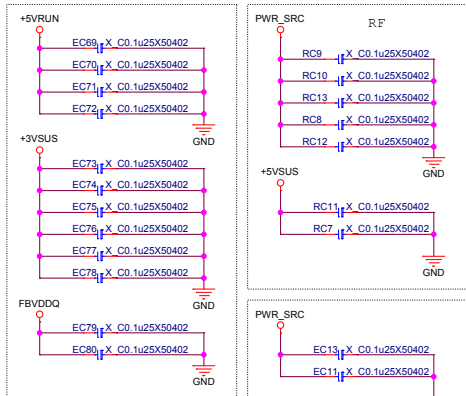
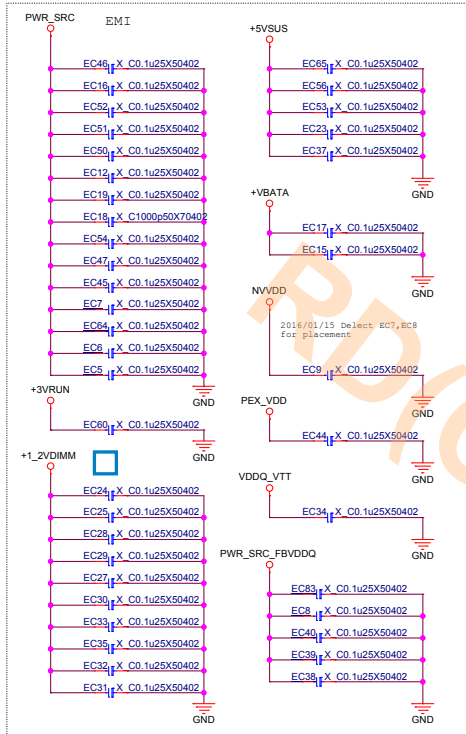




+VCC_CORE
Voltage = Dynamic voltage
Current = Iccmax80A(<10mS)
OCP (typ1) =128A

+VCCGT
Voltage = Dynamic voltage
Current = Iccmax32A(<10mS)
OCP (typ1) =50A





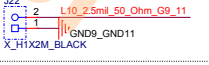
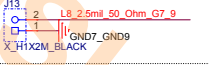
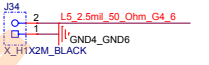
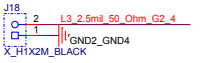
40 OHM Single-End



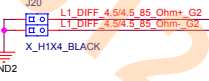
80 OHM Differential



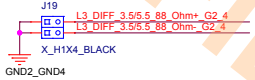
50 OHM Single-End



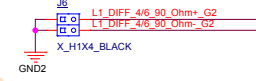
85 OHM Differential



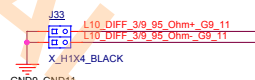
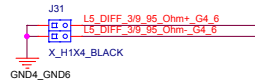
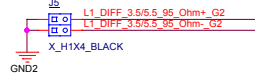
88 OHM Differential



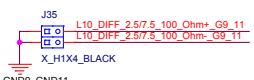
90 OHM Differential



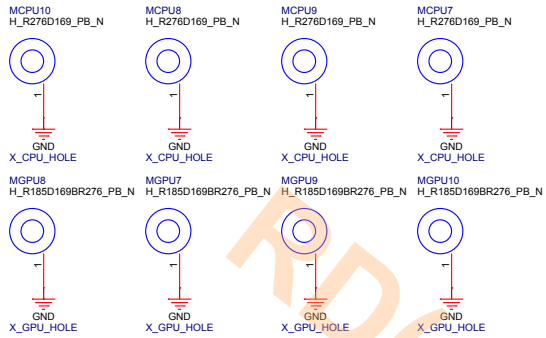
95 OHM Differential



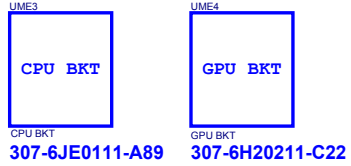
100 OHM Differential



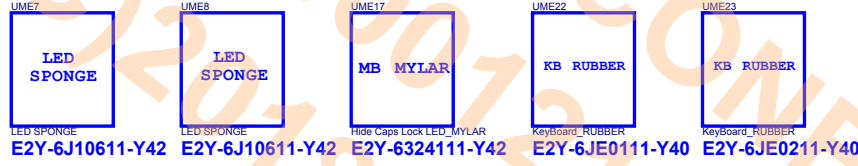
CPU/GPU Holes



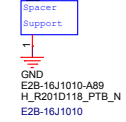
CPU/GPU BRACKET



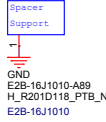
Only 16JE



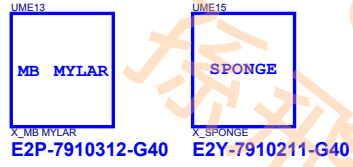
M.2 SSD-1 STAND OFF



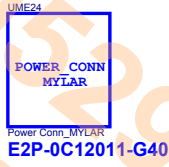
M.2 SSD-2 STAND OFF



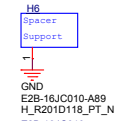
Only 179E



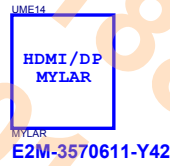
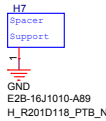
Only ODM



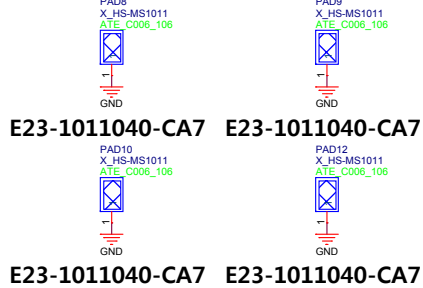
THERMAL STAND OFF



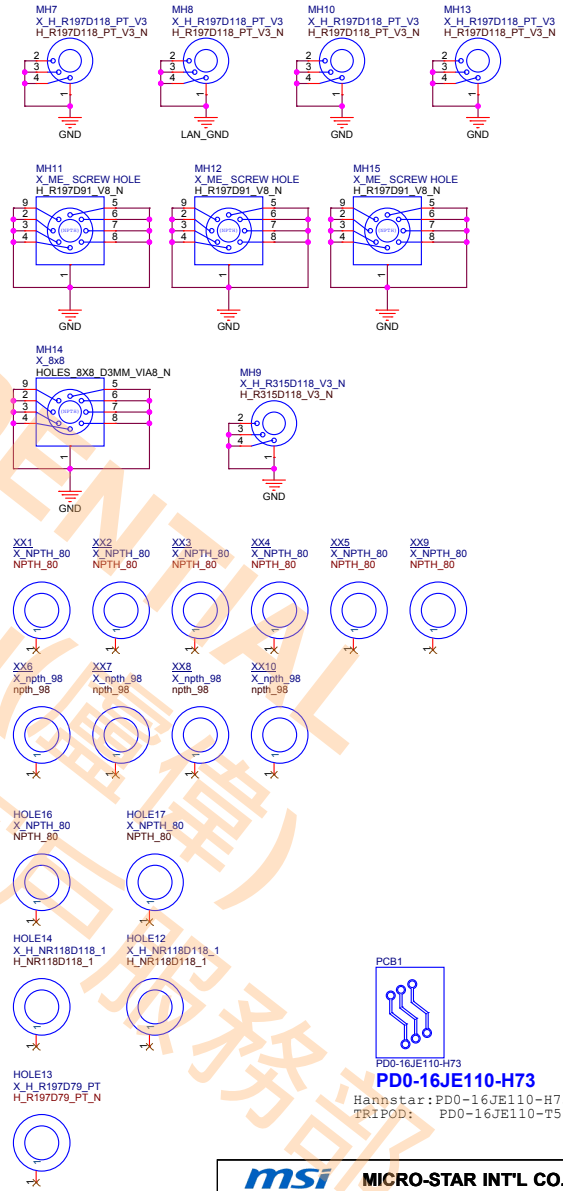
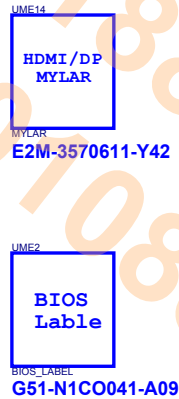
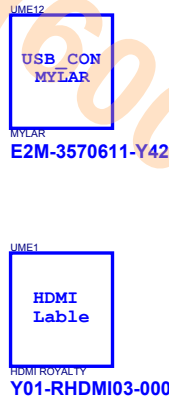
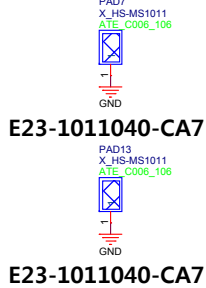
WLAN STAND OFF



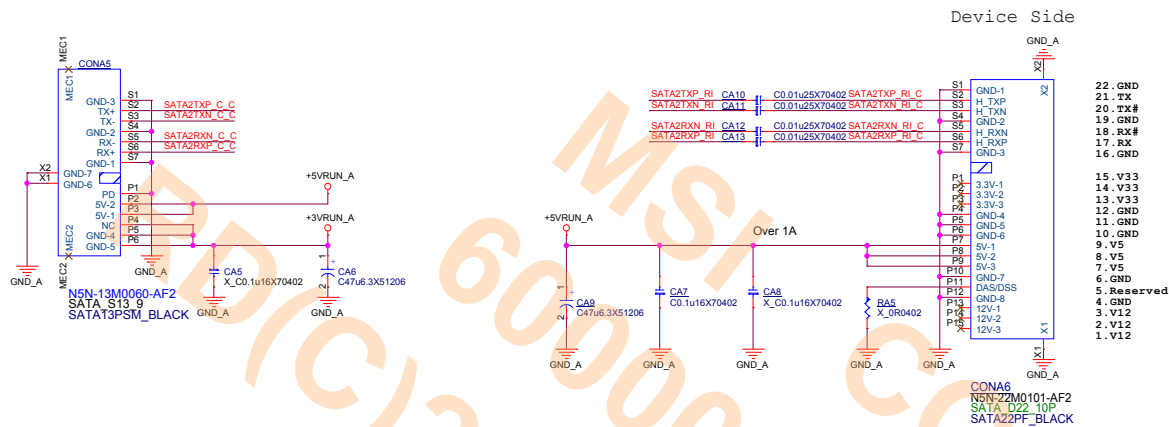
Top Spring



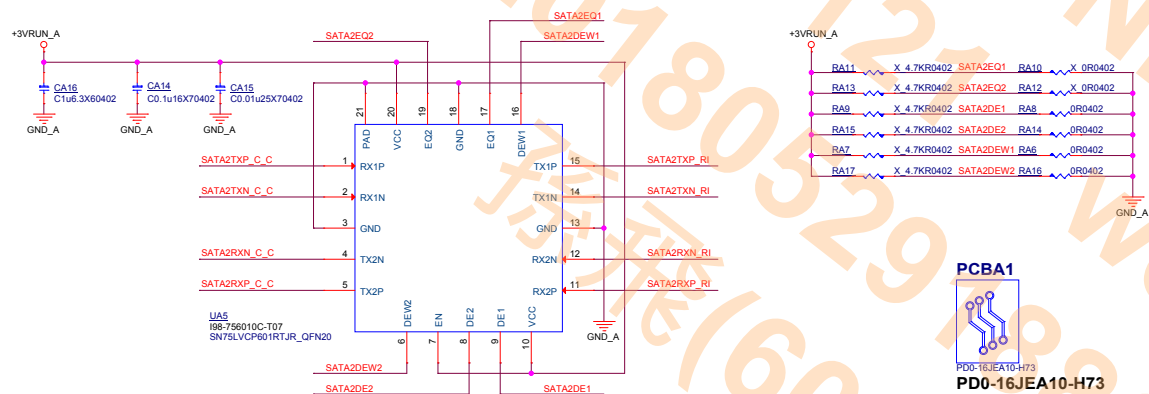
BOT Spring



16JE-A Board (SATA HDD)



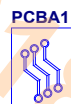
SATA ReDriver



TI SN75LVCP601RTJR HW Setting

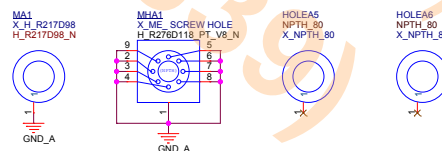
DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2De-Emphasis dB (at 6Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function --> De Width for CH1/CH2
0	De-emphasis Pulse duration, short(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)
1(default)	De-emphasis Pulse duration, long(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)

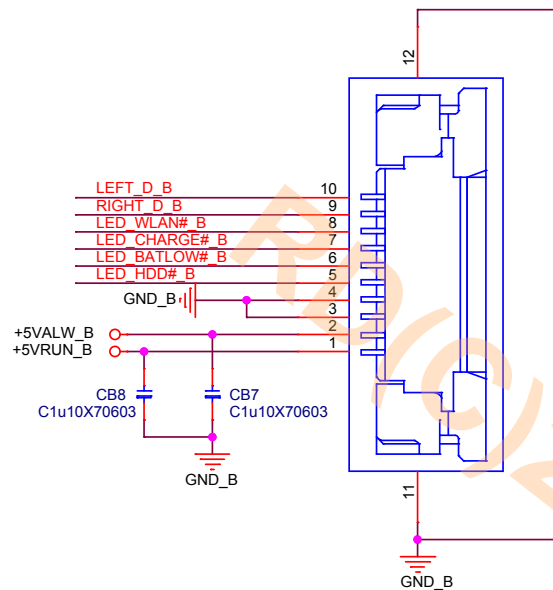


PD0-16JEA10-H73

Hannstar: PD0-16JEA10-H73
TRIPOD: PD0-16JEA10-T53



179E-B Board (LED / TP)



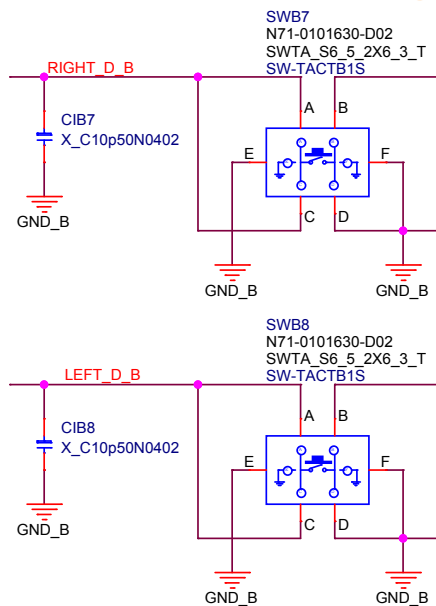
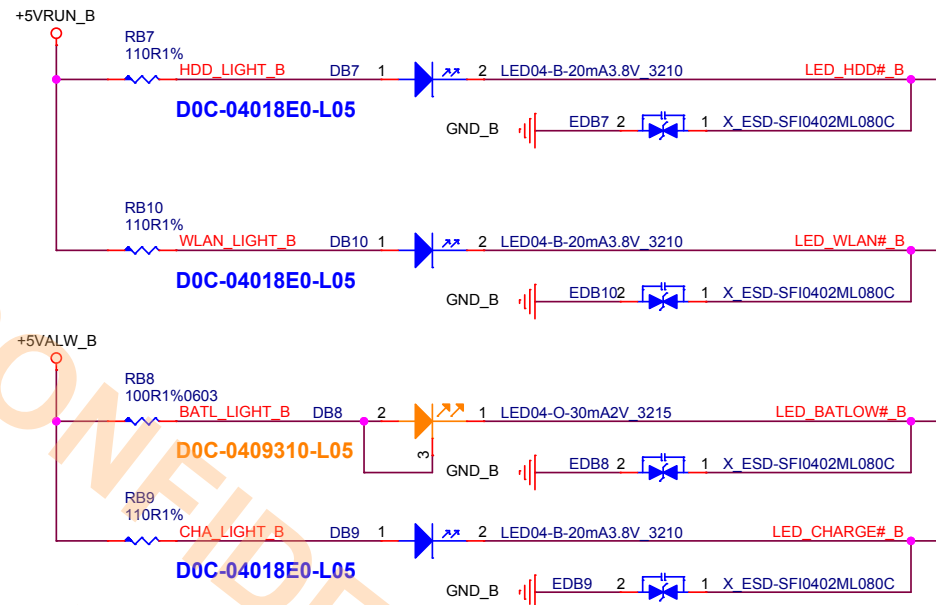
FPCB7
N5A-10F0190-A81
FPC S10.7
FPC70P-B-0.5PITCH_WHITE

LED
BLUE
(HDD)

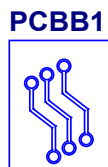
BLUE
(WLAN)

ORANGE
(BATLOW)

BLUE
(CHARGE)




E2P-7910811-G40 E2P-0113511-G40



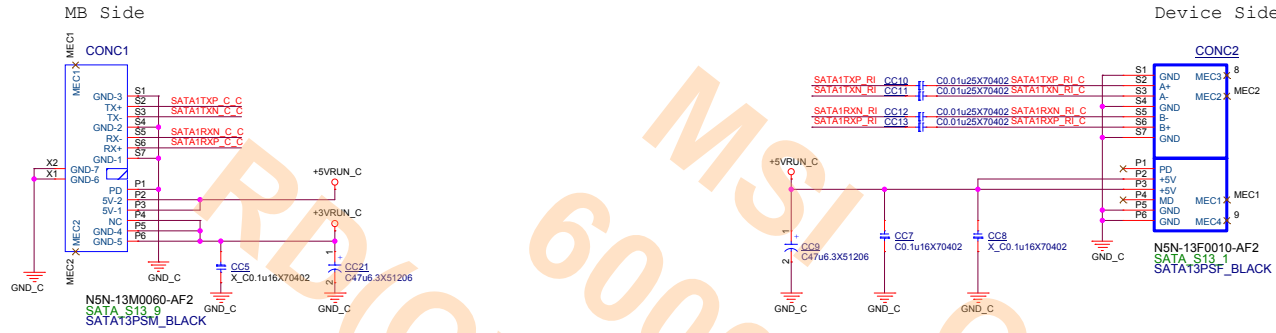
PD0-16JEB10-H73

Hannstar:PD0-16JEB10-H73
TRIPOD: PD0-16JEB10-T53

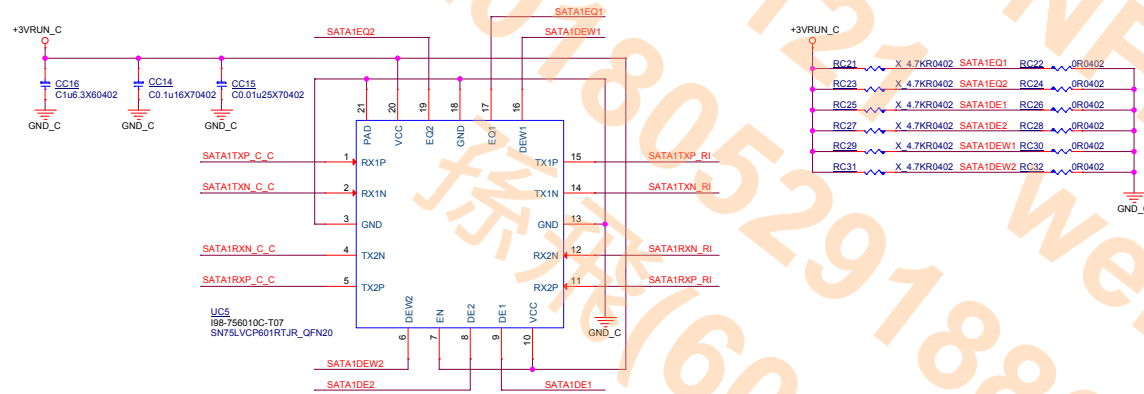


		MICRO-STAR INT'L CO.,LTD.	
Title			
[B] 179E LED/ TP			
Size	Document	Number	Rev
Custom	MS-16JE		1.0
Date:	Monday, December 25, 2017		Sheet 70 of 75

179E-C Board (ODD)



SATA ReDriver



TI SN75LVCP601RTJR HW Setting

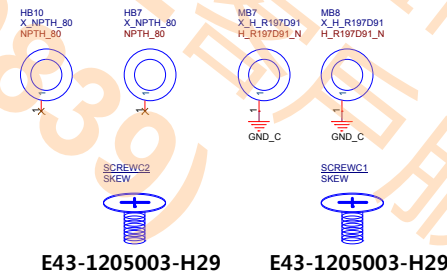
DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2De-Emphasis dB (at 6Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function --> De Width for CH1/CH2
0	De-emphasis Pulse duration, short(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)
1 (default)	De-emphasis Pulse duration, long(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)

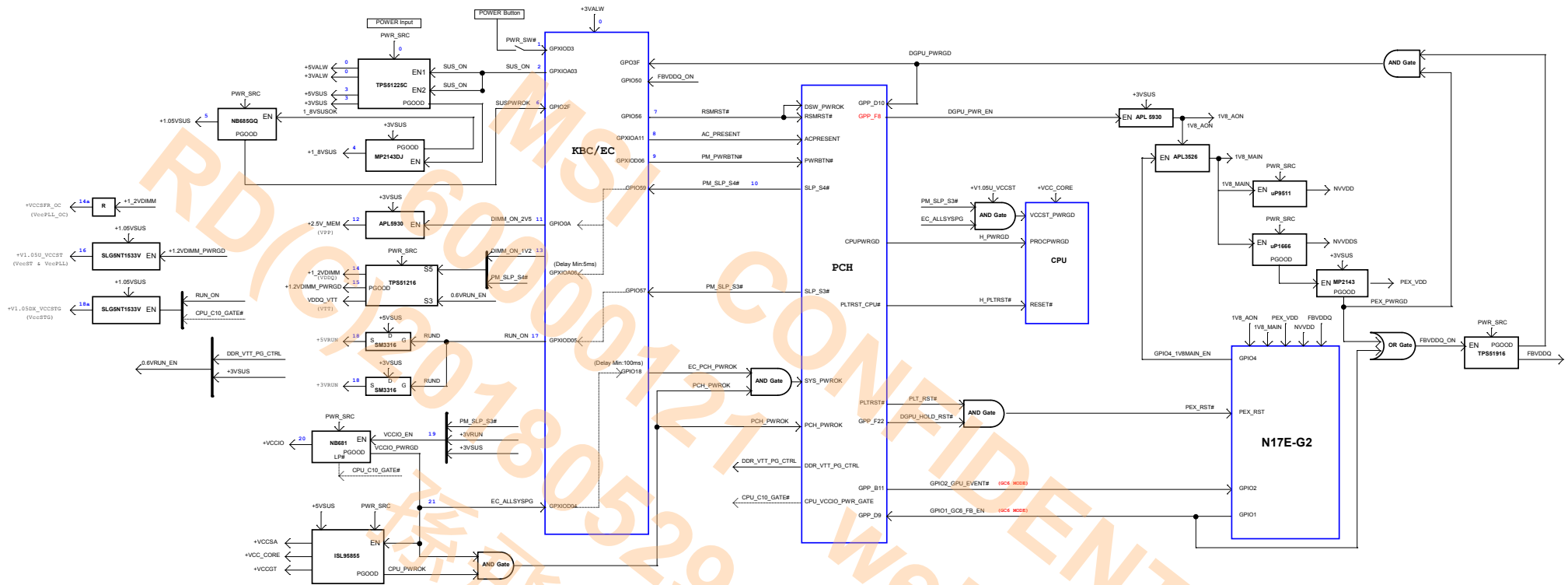
PCBC1



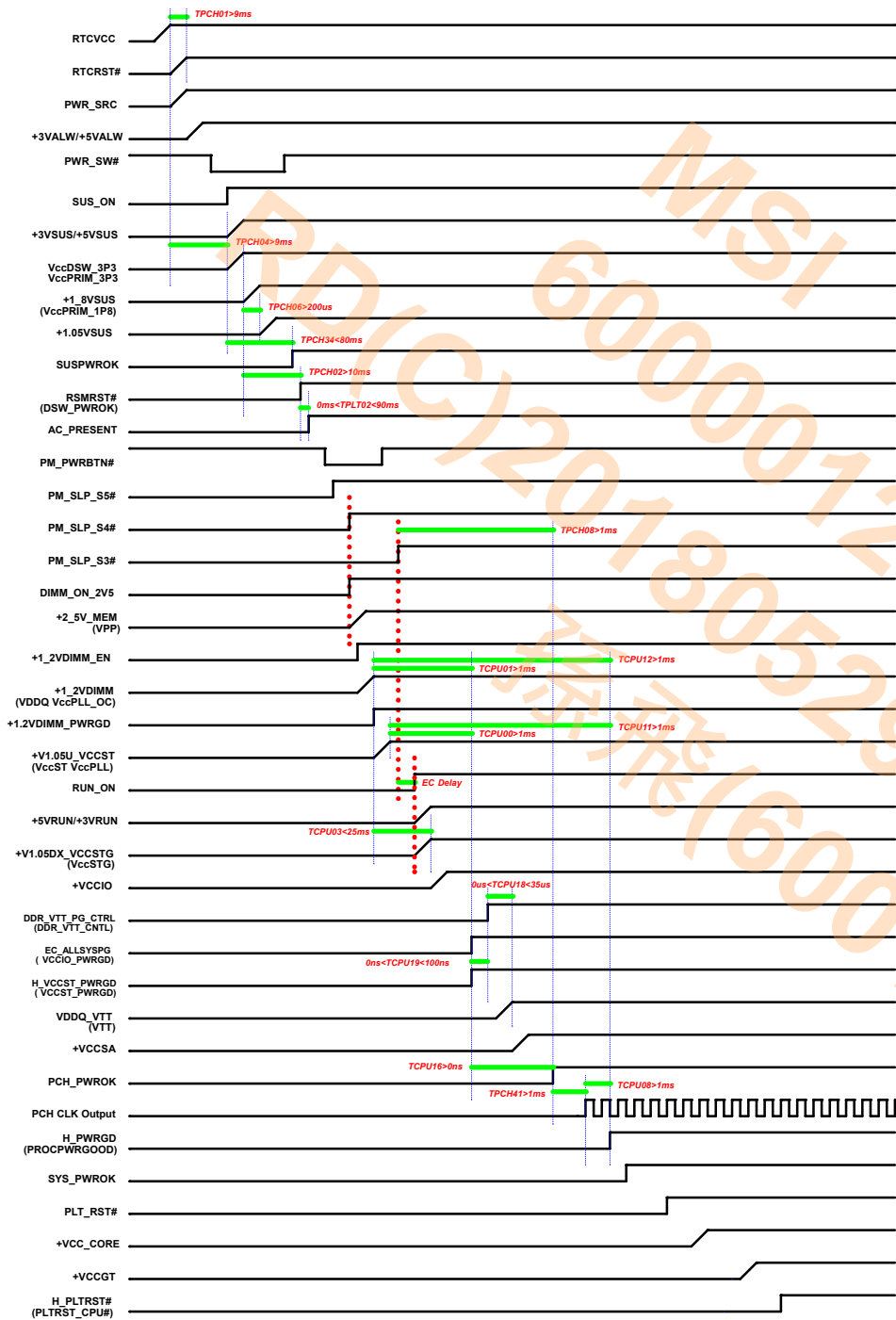
PD0-16JEC10-H73
PD0-16JEC10-H73
 Hannstar: PD0-16JEC10-H73
 TRIPOD: PD0-16JEC10-T53



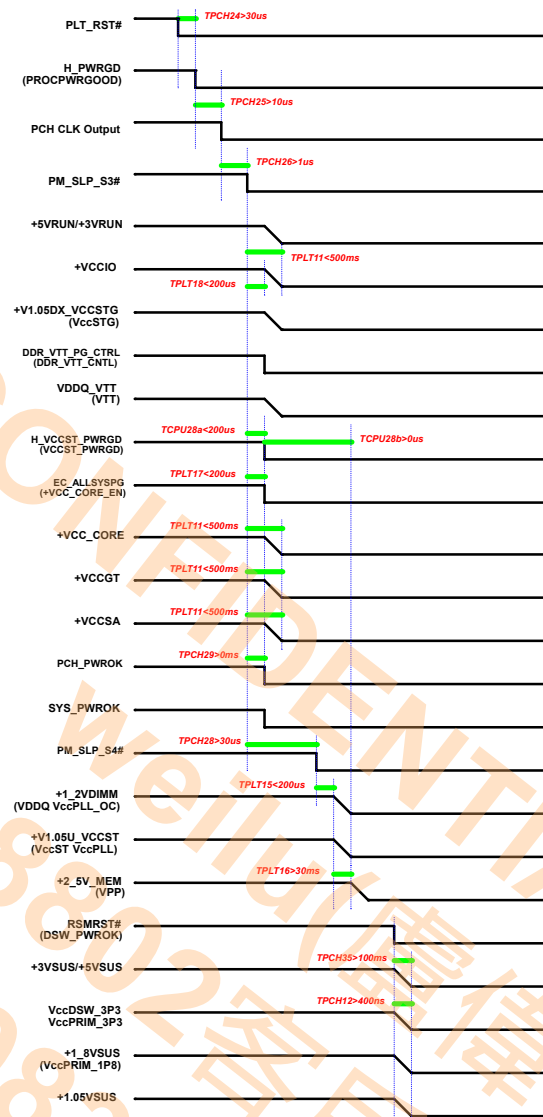
MS-16JE Power on Block Diagram



G3 -> S0



S0 -> G3



History

0A

10

10

Page	Description	Page	Description	Page	Description	Page	Description

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60000121 孫飛(60010839)客戶服務部

